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APPENDIX A

LSI/VLSI ION IMPLANTED GaAs IC PROCESSING

FINAL REPORT FOR THE PERIOD
July 25, 1980 through September 30, 1982

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Rockwell International

APPENDIX A

FEASIBILITY ANALYSIS OF GALLIUM-ARSENIDE MASK PROGRAMMABLE FUNCTIONS AND LOGIC ARRAYS FOR HIGH PERFORMANCE COMMUNICATIONS SYSTEMS

January 12, 1983

FINAL REPORT

Contract No. F49620-80-C-0101 (AFOSR)
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Prepared for

Department of the Army
U.S. Army Electronics Research and Development Command
Fort Monmouth, New Jersey 07703

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1. INTRODUCTION

Circuits critical to the performance of advanced radio, radar and spread spectrum communications systems require advances in the state-of-the-art in semiconductor technology to meet the demands of advanced systems. As these systems increase in complexity, extensive digital circuitry is required in addition to the typical linear signal processing circuits. The power, size and weight of advanced systems also becomes unacceptable without continuous advances in semiconductor technology. Moreover an increasing trend is seen in the use of metal mask selectable functions, programmable logic arrays and gate arrays to implement system specific circuitry in an attempt to lower non-recurring costs, minimize risk and shorten development times. GaAs and other technologies with very high speed power-performance figures-of-merit are critical ingredients in systems implementations which satisfy these needs.

To meet these advanced system requirements this project was initiated as a multi-phase/year program to develop a group of mask programmable gallium arsenide (GaAs) circuit elements applicable to high speed/performance communications systems.

This report covers the activities, performed during Phase I (4 months) of the program, which were initiated to meet the following contract requirements:

1. Generate a kit parts list of circuit elements which could be included in the first mask set to be produced during Phase IIA.
2. Review the list with ERADCOM personnel and prioritize selected elements to be included in the first mask set design.
3. Perform speed/power/size trade-off analysis on different GaAs design approaches and select the one most applicable to systems requirements.
4. Develop preliminary designs of a mask programmable gate array and variable modulus prescalers.
5. Review SYMCAD, (Symbolic Computer Aided Design), and initiate a report on the enhancements/modifications required to use the SYMCAD design methodology for the synthesis and analysis of GaAs circuits. Also, include an estimated time schedule of performance.

2. KIT PARTS LIST

A list of kit parts (Table I), applicable to high performance communication systems, was assembled as a starting point for the selection of circuits to be incorporated within the first mask set to be developed during Phase IIA of this project.

Table 1. KIT PARTS LIST

1. Interconnect and Device Modeling Structures
2. Process Monitor
3. Voltage Controlled Oscillator
4. Mask Programmable Prescalers ÷10/11, 20/21
5. Shift Register
6. Counter with Reset/Preset
7. Up/Down Counter
8. Down Counter with Synchronous Load & Async Clear
9. 4-Bit ALU
10. 4-Bit Accumulator
11. 4-Bit Comparator (< ,=, >)
12. Phase Detector
13. Storage/Logic Array
14. Gate Array

Associated with this list is a selection of satellite systems components (Table II) which could also be used as an aid in the selection of desirable circuits to be developed. Although this table does not list specific circuits per se it does contain fully functional blocks which could be developed using basic kit parts.

A third consideration, contributing to the overall selection of kit parts, was the basic block diagram (Figure 2.1) of a frequency synthesizer. All building blocks within the diagram are listed in Table I excluding the filter.

Table II. SATELLITE SYSTEMS COMPONENTS

1. Multigigabit Devices
   a. R. F. Data Formatters
   b. Modulators
   c. Demodulators
   d. Clock Recovery Circuits
   e. Frequency Synthesizers
   f. Real Time Data Processing
   g. PRN Code Generators

2. Subgigabit Low Power Data Handling Circuits
   a. Signal Routing
   b. Data Formating
   c. Queueing
   d. Data Processing

3. Combination R.F./Digital Circuits
   a. Commandable RF Switch
   b. Pre Amplifiers
   c. Phase Shifters

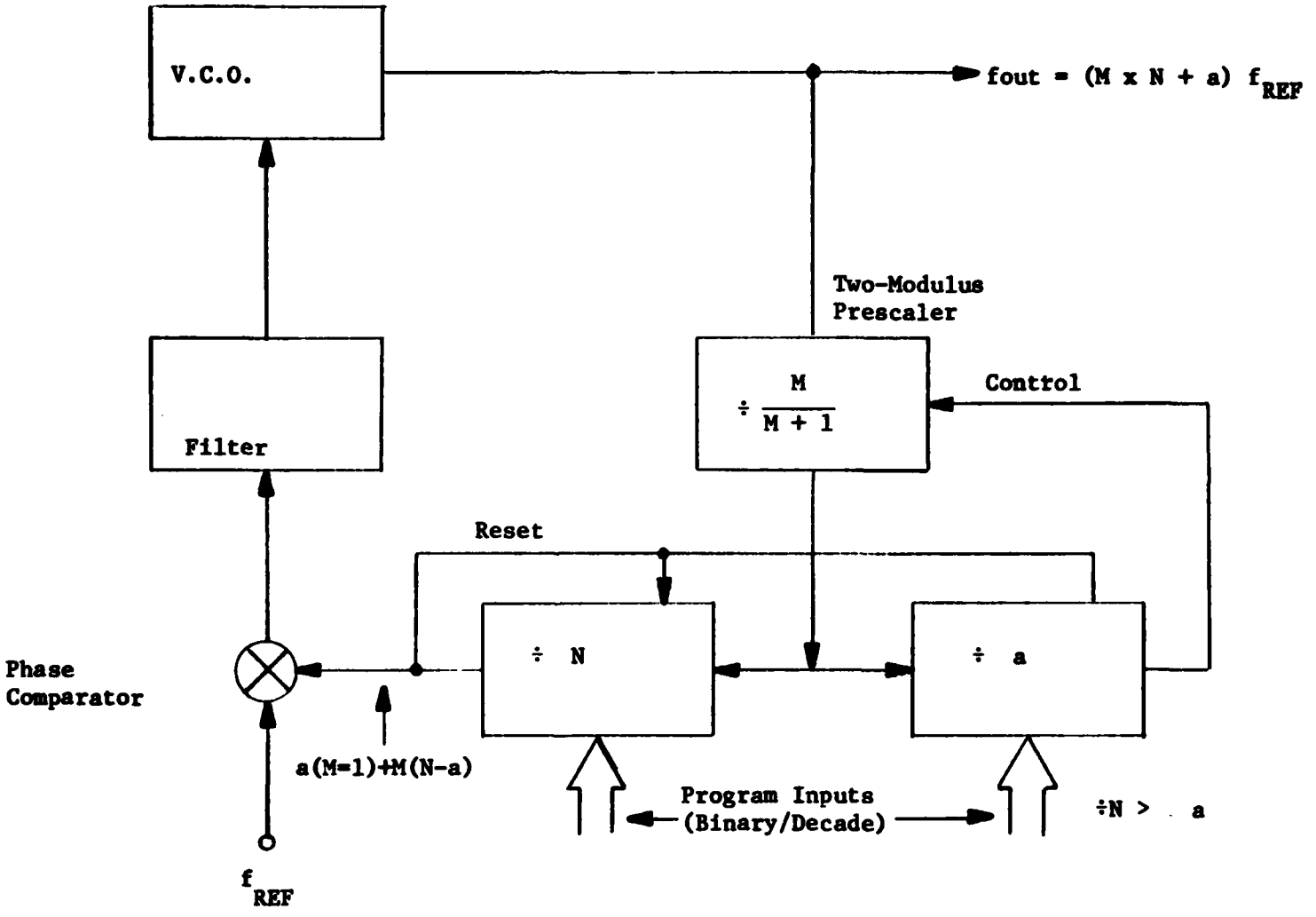


Figure 2.1 Frequency Synthesizer Block Diagram

3. KIT PARTS SELECTION

3.1 Objective

The primary objective of this project is to develop GaAs mask programmable functions and logic arrays suitable for the production of high performance circuit elements applicable to communication systems. This could include both linear and digital circuits, however, at this point in time a joint decision, (ERADCOM-Rockwell), has been reached to limit this project to the implementation of digital functions. The selection of kit parts, to be incorporated within the first mask set using the mask programmable and logic array approach was based on the elements listed in Table I (Kit parts List) of Section 2.

3.2 List Review

In reviewing the list of circuit functions it was decided that the voltage controlled oscillator (Item 3) was not a desirable component to be implemented with the first mask set. The primary objection to this circuit was an expected low signal to noise (S/N) ratio and the fact that most oscillators are designed to meet certain standards of a designated system.

The mask programmable prescalers (Item 4) could not meet all anticipated system requirements, therefore, the list was expanded to provide prescalers with divide ratios of 6/7, 10/11, 20/21 and 40/41.

The counters (Items 6 and 7), along with the 4-Bit ALU, and comparator (Items 9 and 11), were deleted from the list as there was no practical system application for these elements at the present time.

3.3 Kit Parts List

Based on discussions of all data presented to ERADCOM, a prioritized list of (Table III) mask programmable functions to be implemented during Phase IIA of this project was developed.

Although the prescalers in Item 4 are mask programmable, the layout is custom with metal mask options. An alternate approach, storage/logic array (Item 13) or gate array (Item 14) is required to meet most system applications. Of the two choices available it was decided to go with the

storage/logic array which entails a custom flip-flop design associated with cells of uncommitted transistors and diodes.

TABLE III.

PRIORITIZED KIT PARTS LIST

1. Interconnect and device modeling structures
2. Process Monitors
3. Mask programmable prescalers - divide by 6/7, 10/11, 20/21 and 40/41.
4. Phase Detector
5. Binary down counter with synchronous load and asynchronous clear
6. 4 Bit Accumulator
7. Shift Register
8. Pseudo random sequence generator - implemented in a storage/logic array and custom layout if time permits.

4. TRADE OFF ANALYSIS

4.1 APPROACH

Circuit performance trade off analysis was performed using analytical results derived from three (3) independent sources and different MESFET models to select the most appropriate approach for the design of mask programmable functions and logic arrays for implementation of high performance circuit elements applicable to communications systems. One source of analytical data, using a modified SPICE MESFET model, was taken from a Hughes Research Laboratories report, "Study of Gallium-Arsenide and Other Closely Related III-IV Compounds." A second source was from the Rockwell Microelectronics Research and Development Center, (MRDC), Thousand Oaks, Ca. facility where analysis was performed using a modified SPICE MESFET model. The third source of data was appropriated from analysis performed at the Rockwell MRDC Anaheim facility, using a modified JFET transistor as the MESFET model.

4.2 Hughes Research Laboratories Report

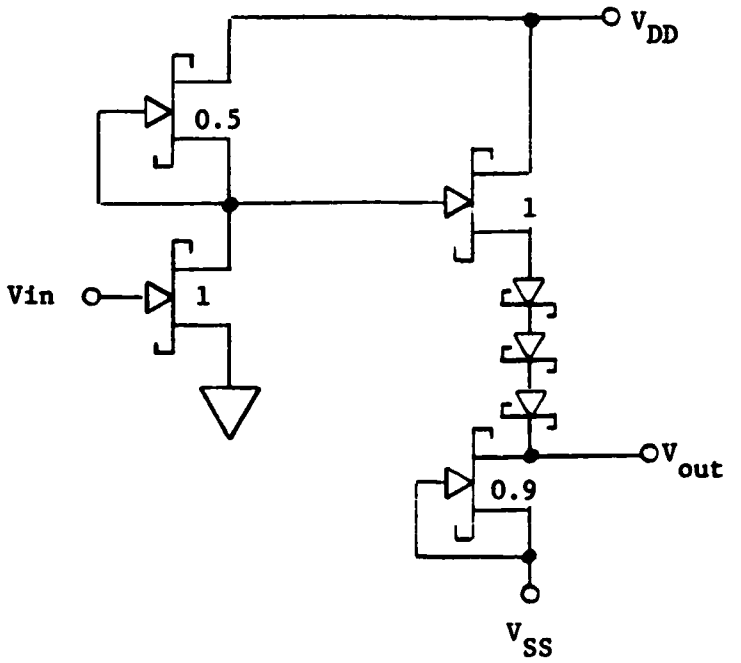
In the final report, "Study of Gallium Arsenide and other closely related III-V Compounds," contract number NB79SBCA, authored by M. Waldner, Hughes Research Laboratories and M. Ercegovac, Computer Sciences Department, University of California Los Angeles, analysis was performed to compare the relative merits of different design approaches to gallium arsenide (GaAs) integrated circuits. Three basic GaAs gate types were analyzed. These include Buffered FET Logic (BFL), Schottky Diode FET Logic (SDFL) and Enhancement Mode FET Logic (ENFL), sometimes referred to as ENFL based Direct Coupled FET Logic (DCFL), as shown in Figure 4.1.

4.2.1 Analytical Model and Performance Parameters

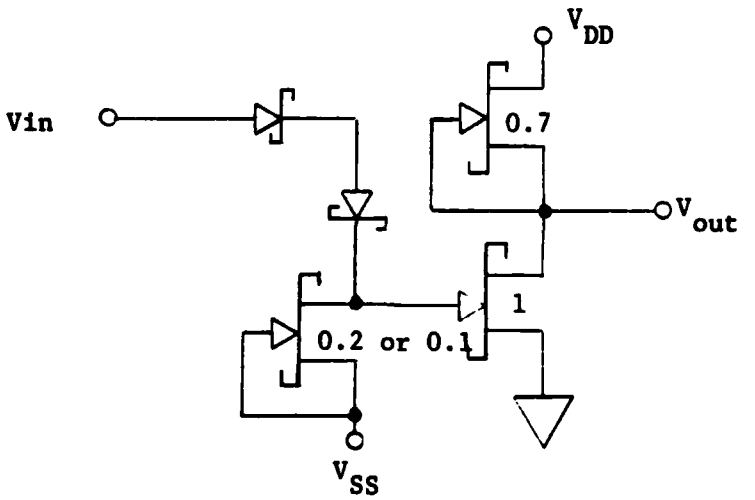
Analysis was performed using the U.C. Berkeley originated circuit analysis program SPICE 2, version 2d. However, the original internal junction FET model was modified to allow an improved fit to the transfer characteristics of GaAs FETS. The circuit performance parameters to be determined by this analysis were:

- o The intrinsic inverter delay for a fan-in and fan-out of one.
- o The additional delay per added fan-in
- o The additional delay per added fan-out
- o The added delay due to the capacitance of inter stage wiring
- o The power dissipation for some standard width of FET

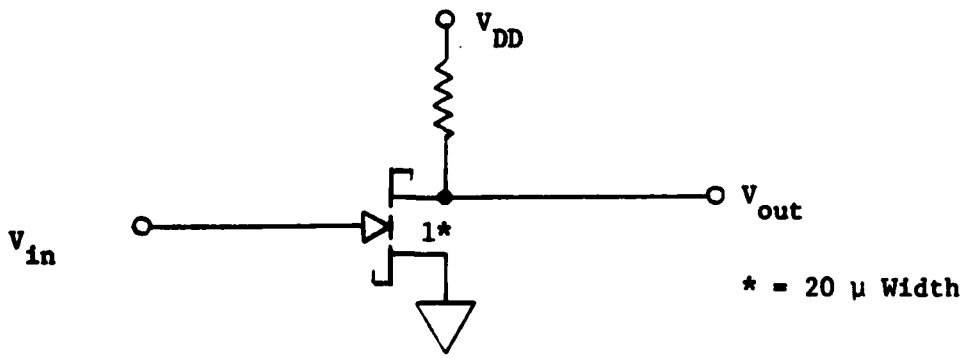
The results are shown in Table IV.



(a) Buffered FET Logic



(b) Schottky Diode FET Logic



(c) Direct Coupled FET Logic

Figure 4.1 Circuit Gate Types analyzed in Hughes Report

Table IV. Characteristics of GaAs Logic Gates from Hughes Comparative Analysis

Calculated Delay	Circuit Type			
	DCFL (Resistive Load), V_{DD} = 0.5	Buffered FET -1V Pinch Off FETs V_{DD} = =3 V_{SS} = -2.5	SDFL Large Pull-Down FET V_{DD} = +2, V_{SS} = -2.5 -0.80 V/FETs	SDFL with Small Pull-Down FET
Basic Inverter Delay (F1 = FO = 1)	170 psec	68	112	150
Extra Delay per Fan Out	106 psec	12.5	95	50.5
Extra Delay per Fan In	23 psec	14.5	23.5	40.5
Extra Delay per mm (or 6E-14F) for 20 μm FETs	121 psec	37	108	90
Power, 20 μm FETs	60 μW	12 mW	2.2 mW	2.0 mW
Power Delay FI = FO = 2, 20μm FETs	17.9 fJ	1.14 pJ	507 Fj	482 fJ

FI = Fan In

FO = Fan Out

A review of the analytical results indicates certain relative attributes/ disadvantages (Table V.), of the different logic gate types when comparing speed, power and area efficiency. These results compare favorably to other analysis found in the literature.

Table V. The Relative Attributes/Disadvantages of Different Logic Gate Types

GATE TYPE	SPEED	POWER	AREA EFFICIENCY
BFL	Highest	Highest	Least
SDFL	< BFL	< BFL	> BFL
DCFL	< SDFL	< SDFL	> SDFL

4.3 Experimental Devices

4.3.1 High Electron Mobility Transistors

With the intense research and development activities on going in the GaAs industry it is expected to see new and novel circuit devices being introduced into the community. One such structure, that has been in the research/development stage for several years, is referred to as a two-dimensional electron gas FET (TEGFET) or high electron mobility transistor (HEMT) shown in Figure 4.2.

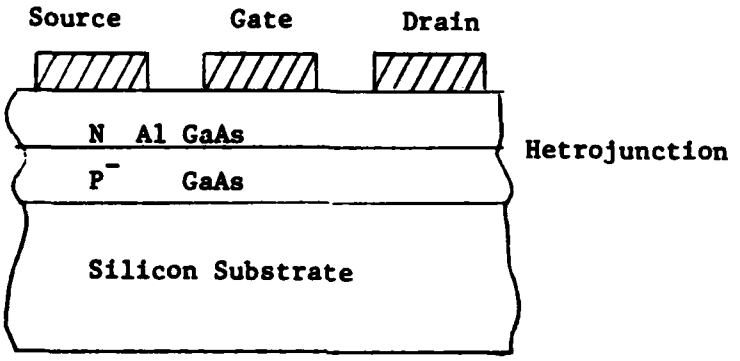


Figure 4.2 Cross-Sectional view of a HEMT

This structure takes advantage of planar molecular beam epitaxy (MBE) processing to develop transistors with extremely high mobilities in the range of 8500, 105,000 and 187,000 $\frac{cm^2}{V\text{-}sec}$ at 300, 77 and 20K respectively. This high mobility is derived in the nonintentionally doped P^- GaAs region where electrons are injected through the hetrojunction formed between the III-V compound interface. Phon N. Tung et-el, of Thomson-CSF Central Research Laboratory, have demonstrated direct coupled FET logic, 11 and 23 stage ring oscillators operating at 300K with 18.4 psec. propagation delays at a power consumption level of 990 μ watt and 32.5 psec at 62 μ watt. In the future they expect that delay times of < 10 psec can be achieved.

4.3.1.1 Rockwell HEMT Devices

Rockwell has also been active in the area of design, processing and testing of HEMT structures. Excellent performance has been obtained from HEMT DCFL (direct-coupled FET logic) ring oscillators recently fabricated. The ring oscillators consisted of nine inverter stages with fan-in and fan-out equal to one. The enhancement-mode switching FETs were 10 μm wide and the depletion mode FET active loads were 4 μm wide, the gate length of the FETs was 1 μm and the source to drain spacing was 4 μm. Two separate Schottky layers were used to fabricate the enhancement mode FETs and the depletion mode FETs; proton bombardment was used for device isolation. These are the first HEMT circuits fabricated with a planar structure as opposed to the mesa structure used at Fujitsu and Thomson CSF.

The performances of the ring oscillators were measured as a function of the supply voltage, V_{DD}. A typical result is shown in Fig. 4.3. The propagation delay time (τ) decreases as V_{DD} is increased from 0.7 V to 1 V, and stays constant at about 44 ps when V_{DD} is increased above 1 V. The speed-power product (P_τ) increases linearly with V_{DD}, indicating that the current level at which the circuit operates stays constant. The highest speed obtained at room temperature was 36.6 ps and the lowest speed-power product was 2.43 fJ. Such performance is the best ever reported for 10 μm wide devices. Although the speed is not as high as that of ring oscillators with devices (> 20 μm) as reported by Fujitsu and Thomson CSF, the speed-power product is about the same or lower than their values. If the width of the FETs is increased and the device design is improved by reducing the source to drain spacing, a significant improvement in circuit speed should be observed.

The long development cycle from research to pilot line production negates these devices being on line within the time frame of this program, however, it is projected that circuits using the HEMT structure will be available from our pilot line production facility in 1985.

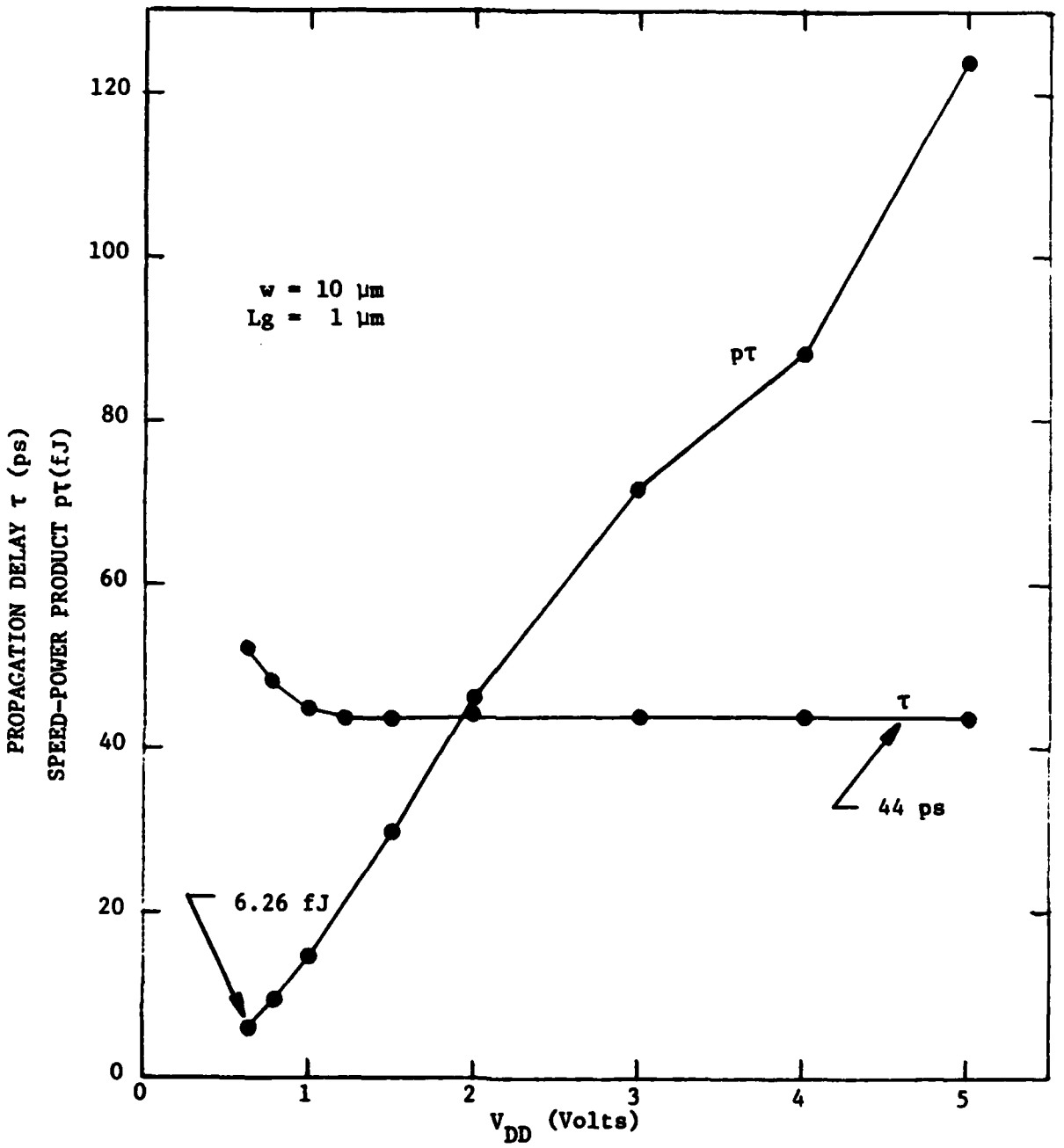


Figure 4.3 Speed-Power Performance of A HEMT E/D Ring Oscillator

4.3.2 Enhancement Mode MESFET

The introduction of enhancement mode (E-Mode) MESFET's along with the available depletion mode (D-Mode) devices, into the circuit designers arena, offers a chance to develop high speed low power circuits that are area efficient, require no level shifters and are truly digital in nature. Many companies have been actively involved in the research/development of planar processing applicable to the production of both E-Mode and D-Mode transistors on the same circuit. This is evidenced by papers presented at the 1982 GaAs IC Symposium in New Orleans and also in the published literature. With the availability of both structures, GaAs VLSI circuits operating at GHz clock rates and dissipating a few hundred milli-watts of power, will be a reality.

4.3.2.1 Rockwell E/D MESFETS

Experimental work has been performed towards development of ion implanted enhancement mode devices compatible with our present depletion mode planar process (Figure 4.5). The E-Mode devices were fabricated using a recessed gate technique. Using the E/D transistors, direct coupled FET logic (DCFL) ring oscillators were produced and evaluated.

A typical example of the circuit speed versus supply voltage, V_{DD}, is shown in Figure 4.4 The propagation delay varies from about 100 ps to 80ps, and the speed-power product increases linearly when V_{DD} is changed from 0.7 to 5 V. Comparing this performance with that of a HEMT shown in Fig. 4.3, the ion implanted ring oscillator operates at a much lower speed but a lower power consumption than the HEMT ring oscillator does. The superior speed performance of the HEMT circuits is mainly due to the higher transconductance of the HEMT devices.

Although these basic experiments indicate that a viable E/D mode transistor process is feasible, Rockwell does not intend to pursue their development at the present time.

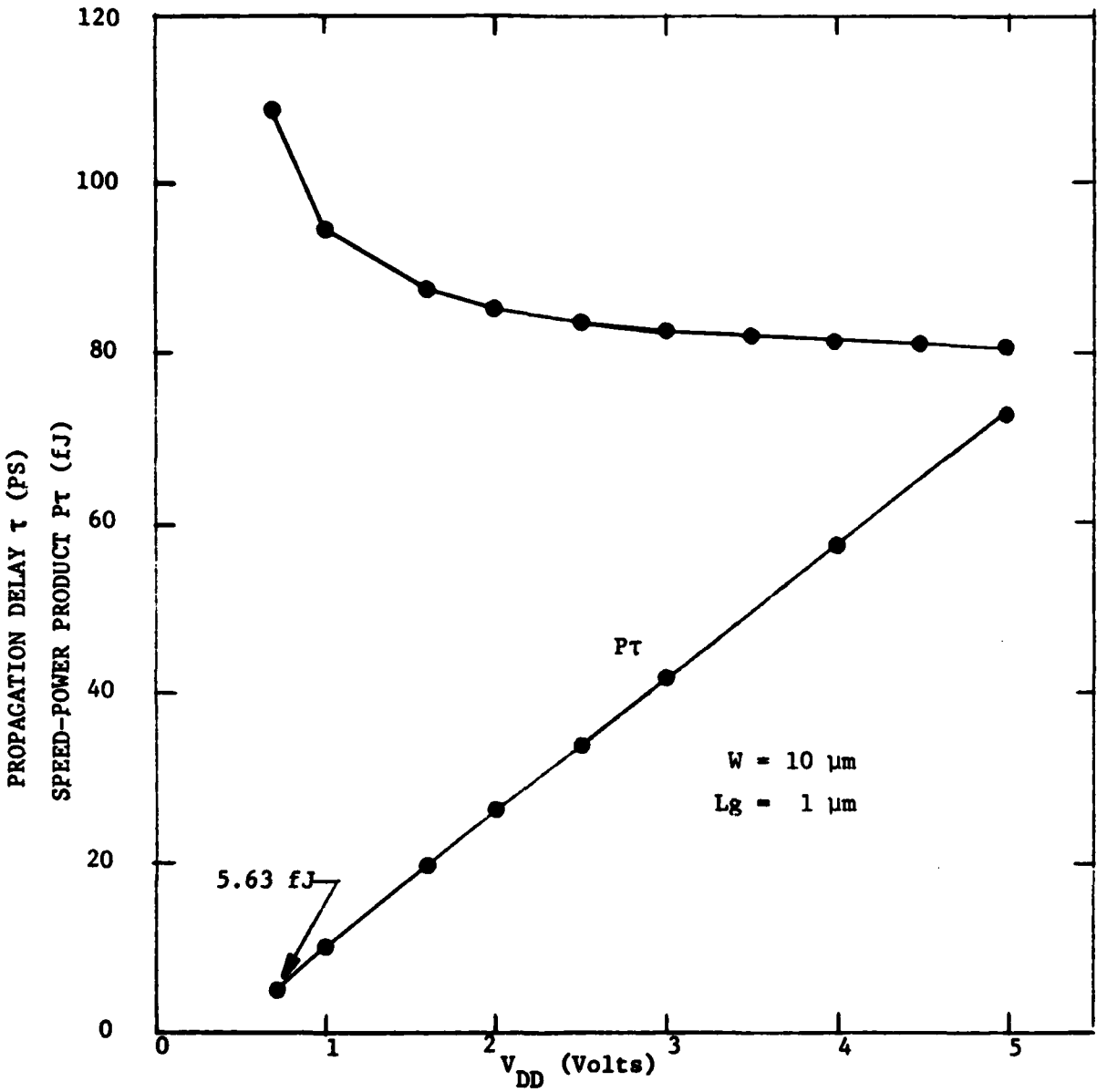


Figure 4.4 Speed-Power Performance of an Ion-Implanted E/D Ring Oscillator

4.4 Available Circuit Components and Gate Types

With the present on-line GaAs planar process (Figure 4.5), at the Rockwell pilot line facility, circuit components are limited to depletion mode MESFET's, Schottky diodes and saturated resistors. Under these constraints the enhancement mode MESFET is not available for the design of very low power enhancement/depletion (E/D) mode circuits. Therefore, attention will be focused on circuit implementation based on two of the three basic gate types analyzed in Section 4.2.

4.4.1 Gate Types

Two recognized standard gate types which can be produced, using the available components, include buffered FET logic (BFL) and Schottky diode FET logic (SDFL). Modifications can be made to these devices to ameliarate some of their more objectional characteristics such as the output loading problems associated with SDFL and the higher power requirements of BFL.

4.4.2 BFL NOR-Gate

A standard two-input BFL NOR-gate, as shown in Figrue 4.6 (a), can be modified to reduce total power per stage by the removal of the output buffer transistor (Figure 4.6 (b). This un-buffered FET logic (FL) has two distinct advantages:

- o Reduces Power Requirements
- o Reduces Area Requirements

The obvious disadvantages of this approach is the circuit loading sensitivity. In the design of gate types available for gate array structures, the basic cell could be designed as buffered FET logic with the ability to remove the buffer, using mask programming techniques, if the local load environment does not demand a strong driver stage. Although this approach does not represent a savings in area it will help reduce overall power requirements. A combination of BFL and FL gate structures could be used in an optimized circuit design taking advantage of the flexibility offered.

4.4.3 SDFL NOR-Gate

The Schottky diode FET logic (SDFL) two-input NOR-gate, as shown in Figure 4.7 (a), is considered a moderate speed/power circuit approach for implementation of digital functions. However, the technique is inflexible with respect to output loading, (the output circuit must be tailored to its

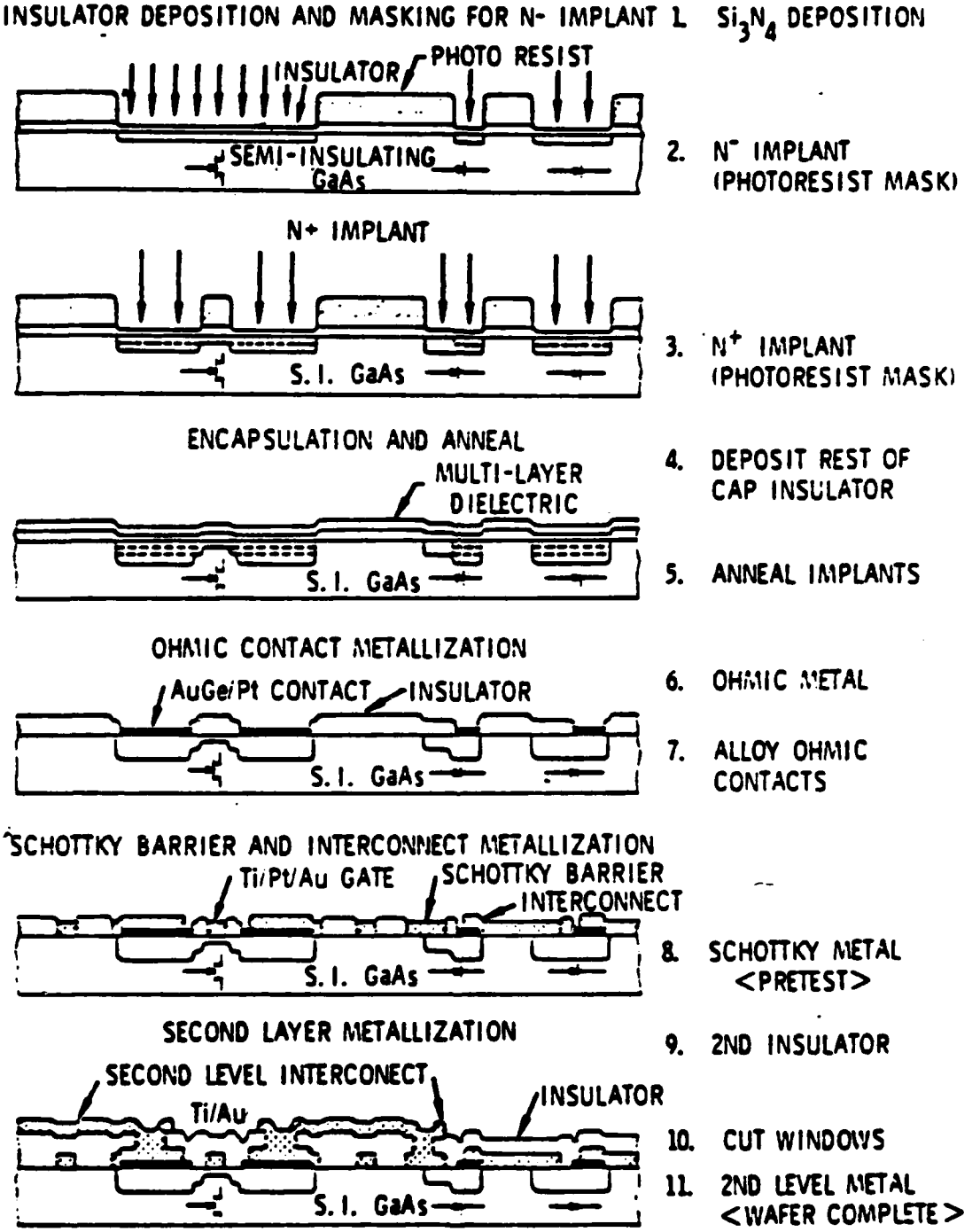
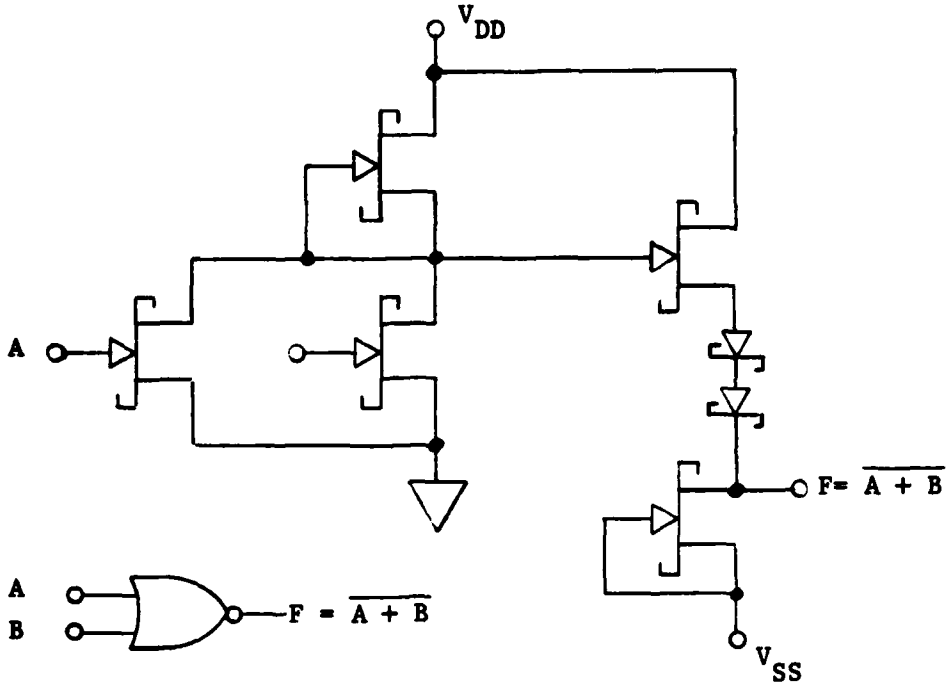
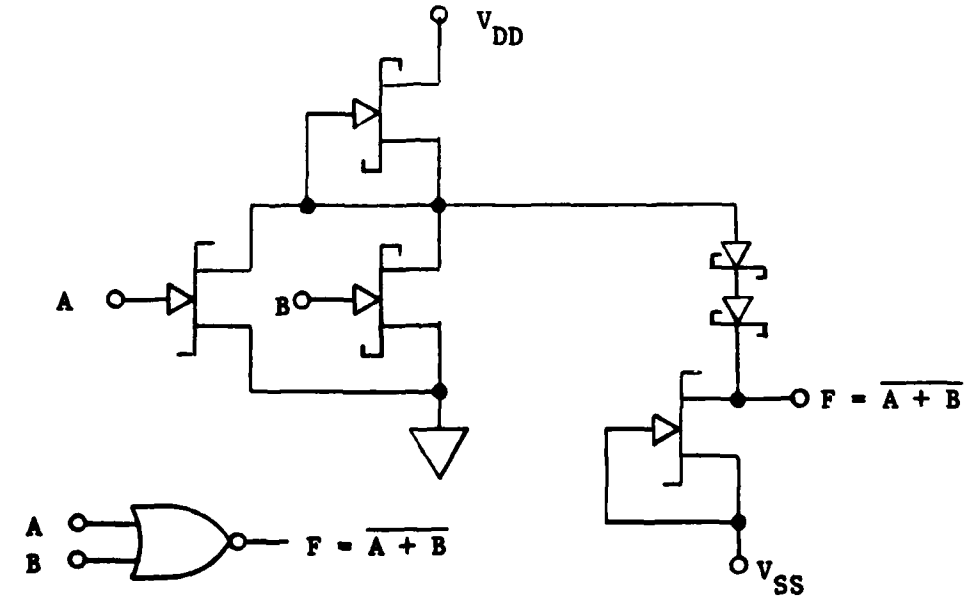


Figure 4.5 **Planar GaAs IC fabrication steps.**

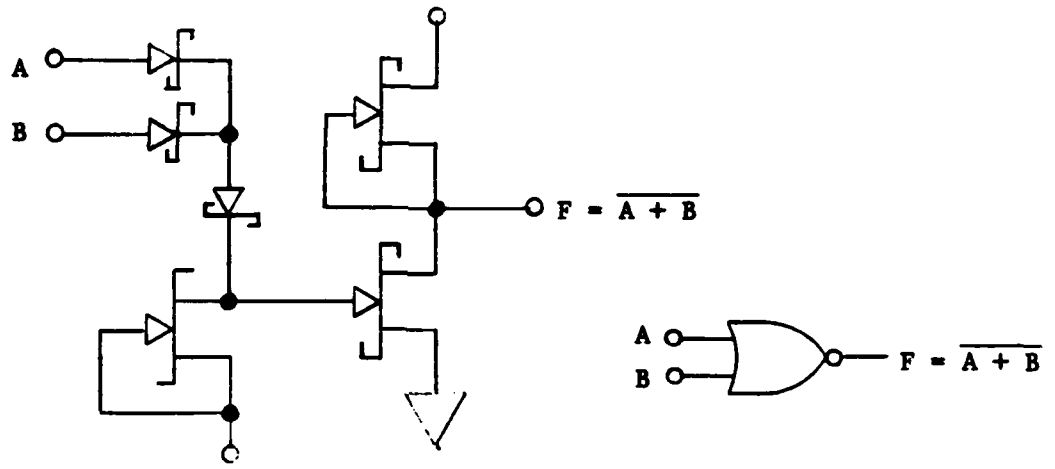


(a) Buffered Fet Logic (BFL)

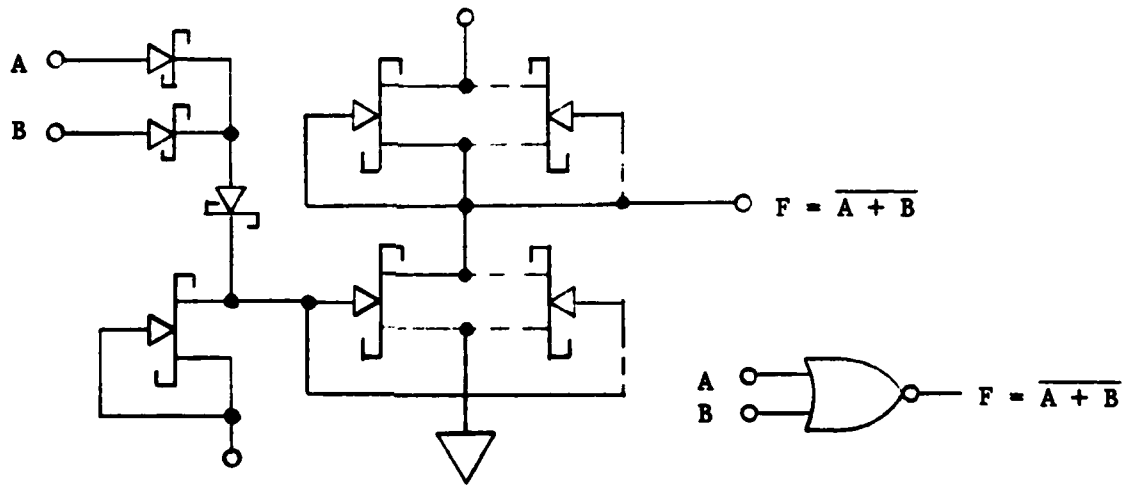


(b) Un-buffered Fet Logic (FL)

Figure 4.6 BFL and FL Two-Input NOR-Gates



(a) Schottky Diode Fet Logic (SDFL)



(b) Programmable Schottky Diode Fet Logic (PSDFL)

Figure 4.7 SDFL and PSDFL Two-Input NOR-Gate

load). An approach to make SDFL more flexible for gate array designs is the addition of an auxiliary output transistor pair which could be wired in parallel, with mask programming, to the original circuit (Figure 4.7 (b). This approach allows construction of logic functions with minimum transistor sizes with reduced power in a localized area and at the same time it provides a buffer which can be wired in at any time to drive increased loading requirements. One problem associated with this approach is the design of the input circuit including the pull-down transistor which must respond to the extra loading when the auxiliary transistor pair is required.

4.5 Comparative Speed/Power Analysis of FL, SDFL and PSDFL

Speed/Power analysis was performed using a three stage ring oscillator (Figure 4.8) as the test vehicle. The circuit elements were multiple input NOR-gates, connected as inverters, implemented with FET logic (FL), Figure 4.9, Schottky diode FET logic (SDFL) and programmable Schottky diode FET logic (PSDFL), Figure 4.10. The transistor/diode sizes, used to construct the FL, SDFL and PSDFL gate structures, are listed in Tables VI and VII. A matrix of nine (9) test cases were run, for each gate type, with capacitive loading of 20, 50, and 100 femto-farads (fF) and fan-outs of 1, 2 and 3. The MESFET and diode models used in this analysis were modified versions of JFET and diode models contained within the general-purpose circuit simulation program SPICE II (Version 2E.2), which was developed by the integrated circuits group at the University of California, Berkeley, and installed on Rockwell's CYBER 176 computer at the Microelectronics Research and Development Center, Thousand Oaks facility. The results of the analysis are listed in Table VIII. It should be noted that the power dissipation per gate remains constant as the current is limited due to the associated transistors operating in the saturated mode. With limited current source/sink capabilities the gate propagation delay will increase in relationship to the capacitive loading.

4.5.1 Review of Analytical Results

A review of the analysis (Table VIII), indicates a decided edge for SDFL when comparing gate propagation delay and power dissipation. A hidden problem shows up when the output voltage swing is considered. A voltage difference of 1 volt, (0.7V to 1.7V), would make the circuit useless under worst case loading conditions. The remaining circuit approaches, (FL and SDFL), do not show an

over-powering case for either approach. A switch over between the two cases appears when the capacitive load is 50 fF with a fan-out of 2. Beyond this point the PSDFL takes over. This may indicate a case for the use of buffered FET logic (BFL) when loading is above a certain level. Another qualifier, as to the soundness of a certain approach, is the power-delay, (femto-joules), figure of merit. As shown in Table IX SDFL wins without a doubt, however, it has been deleted for consideration by other reasons. Of the remaining choices the obvious would be FET logic (FL).

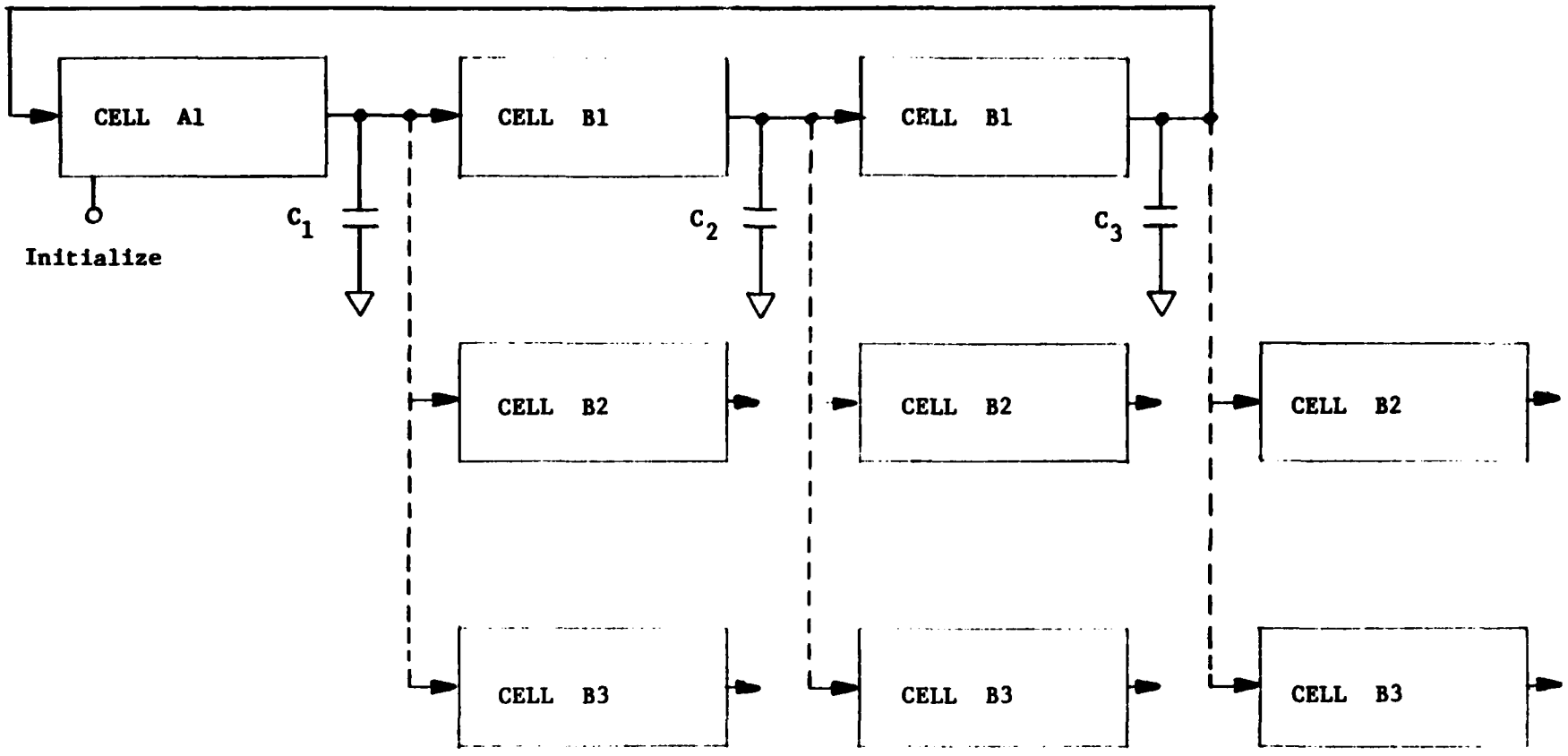
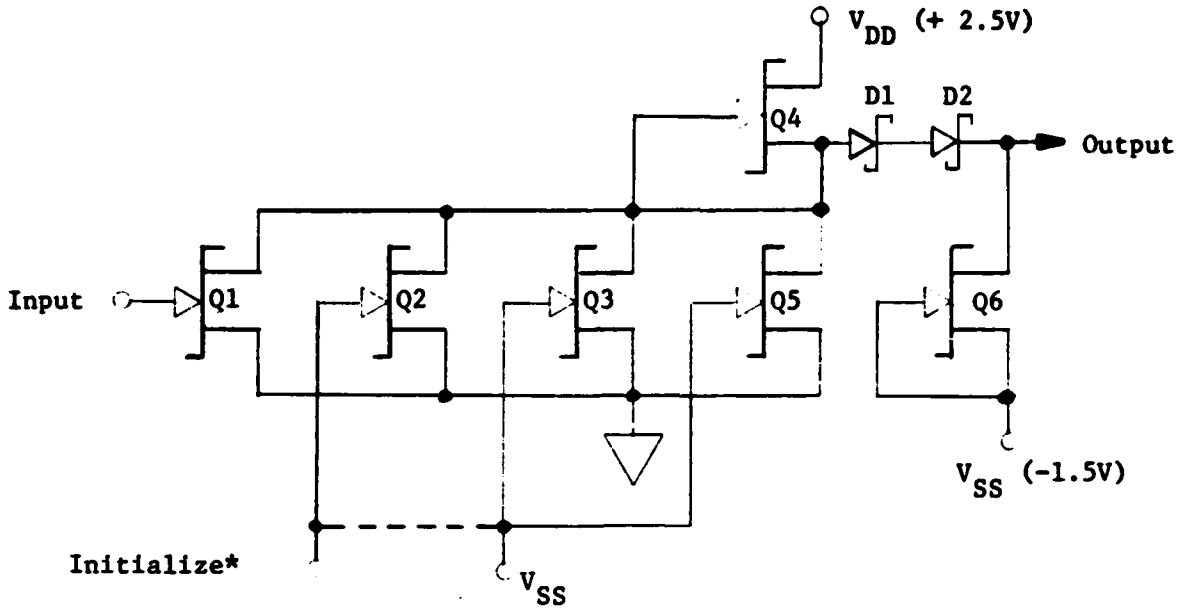


Figure 4.8 Block Diagram of 3 Stage Ring Oscillator used for Comparative Speed/Power Analysis.

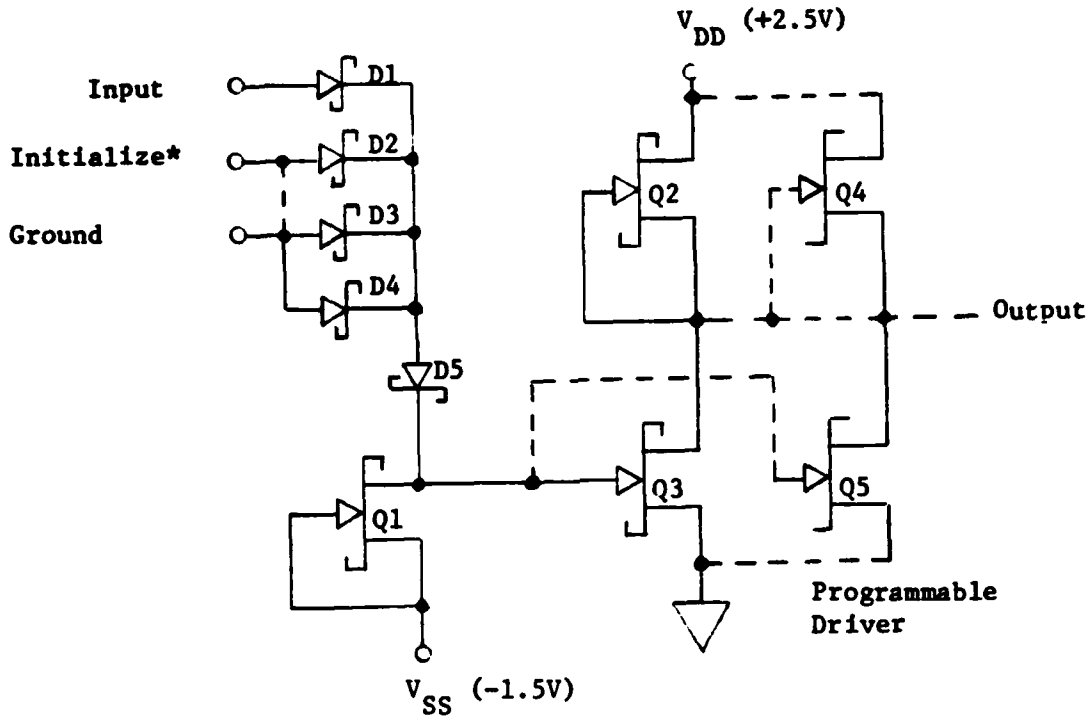


* In Cell B Initialize is tied to V_{SS}

Figure 4.9 FL Cell A and B Design

Table VI FL Transistor/Diode Dimension

Transistor	Width (Microns)	Dimensions (Microns)	Gate Length (Microns)
Q 1	10		1
Q 2	10		1
Q 3	10		1
Q 4	10		1
Q 5	10		1
Q 6	5		1
Diode			
D 1		2 x 5	
D 2		2 x 5	



* In Cell B Initialize is tied to ground

Figure 4.10 SDFL Cell A and B Design

Table VII. SDFL Transistor/Diode Dimensions

Diodes	Dimensions (Microns)	Width (Microns)	Gate Length (Microns)
D1,D2,D3,D4	1 x 2		
D5	2 x 3.5		
Transistors			
Q1		2.5	1
Q2,Q3,Q4,Q5		10.0	1

Table VIII. Results of 3 Stage Ring Oscillator Analysis

CIRCUIT LOADING		GATE PROPAGATION DELAY (Ps)			POWER DISSIPATION/Gate (mw)			OUTPUT AMPLITUDE (Volts)		
FAN OUT	CAP LOADING (fF)	FL	SDFL	PSDFL	FL	SDFL	PSDFL	FL	SDFL	PSDFL
1	20*	153	128	215	1.8	1.1	2.1	1.1	1.7	1.9
2	20	193	160	228	1.8	1.1	2.1	1.0	1.4	1.7
3	20	233	190	238	1.8	1.1	2.1	0.9	0.7	1.6
1	50	215	173	230	1.8	1.1	2.1	1.1	1.7	1.9
2	50	258	220	245	1.8	1.1	2.1	1.0	1.4	1.7
3	50	303	255	255	1.8	1.1	2.1	0.9	0.7	1.6
1	100	323	253	258	1.8	1.1	2.1	1.1	1.7	1.9
2	100	368	320	273	1.8	1.1	2.1	1.0	1.4	1.7
3	100	438	360	288	1.8	1.1	2.1	0.9	0.7	1.6

* 1fF ≈11 μm wire run

Table IX Power - Delay Comparison

CIRCUIT LOADING		[Power (mw)] • [delay (ps)] femto-joules (fj)		
FAN OUT	CAP LOADING (fF)	FL	SDFL	PSDFL
1	20	275	141	452
2	20	347	176	479
3	20	419	209	500
1	50	311	190	483
2	50	396	242	515
3	50	459	281	536
1	100	455	278	542
2	100	576	352	573
3	100	648	396	605

4.6 Gate Type Selection for Gate Array Application

As the analysis in Section 4.5 and 4.6 indicate, there is not a preponderance of evidence to support the choice of BFL over SDFL. However, since the main objective of this program is to develop mask programmable functions and logic arrays we must assess the intrinsic aspects of the various logic forms in view of their application. Therefore, a review of the fundamental operational characteristics of the gate types is appropriate at this point in time.

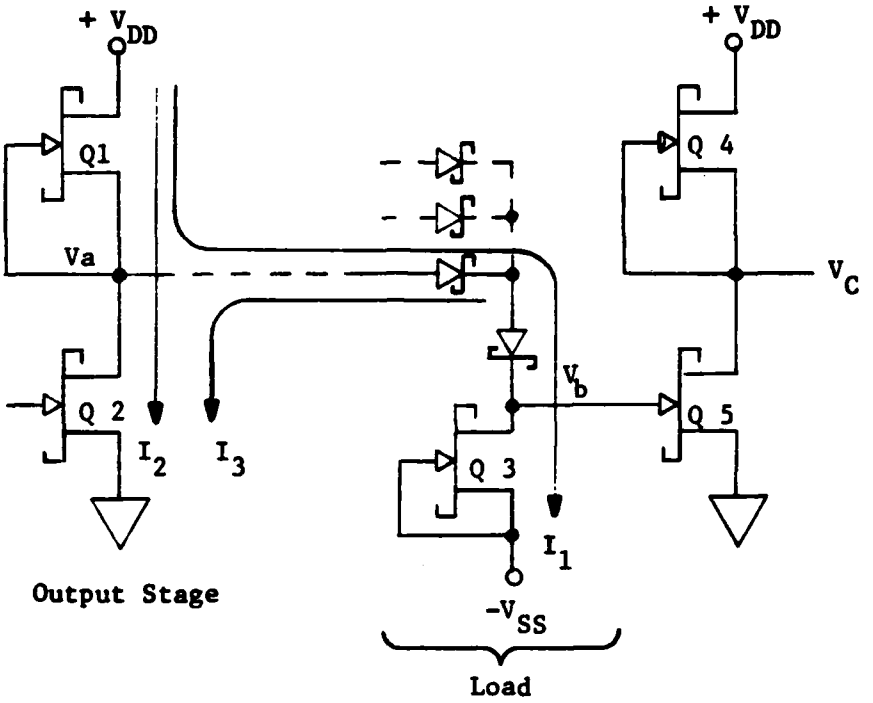


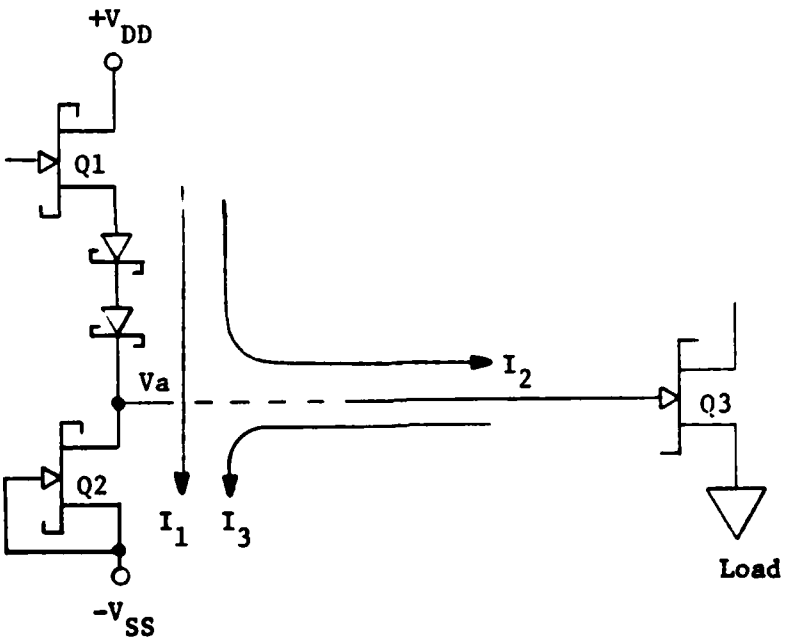
Figure 4.11 SDFL Output Stage and Associated Load

4.6.1 SDFL Characteristics

Figure 4.11 shows an SDFL output stage and associated load. The output circuit from a remote stage (Q1 and Q2) must supply a current I_1 to the input circuit of a gate when transistor Q_2 is cutoff. This current must be sufficient to produce voltage drops across all series elements to insure that the voltage V_b is approximately 0 volts. Deviation from this point will cause variations in the Q5 on-resistance thereby shifting the output voltage V_c which must in turn feed another gate. When transistor Q2 is turned on

currents I_2 and I_3 will flow. I_2 is a continuous (DC) current setting up a voltage division between Q1 and Q2 which produces the voltage Va. With this point near 0 volts the diodes become back biased and V_b approaches the voltage $-V_{SS}$. The point that should be made clear is the fact that in custom designed circuits the transistors and diodes can be scaled to meet load requirements. This cannot be done readily in a gate arrays where the functions being implemented and the loading are unknown at the time of the gate array design. Improperly scaled structures would cause a catastrophic failure (Inoperative circuits).

4.6.2 BFL Characteristics



Output Stage

Figure 4.12 BFL Output Stage and Associated Load

Buffered FET logic (Figure 4.12) requires a level shifter as does the SDFL approach. However in the case of BFL the level shifter is combined with the output circuit transistor to form a local area source/sink capability. When transistor Q1 is turned on a DC current I_1 flows from $+V_{DD}$ to $-V_{SS}$ setting up the voltage Va and at the same time a transient current (I_2) is sourced to charge up all line and device capacity connected to the output terminal. In the steady state, (if we ignore leakage currents) only the DC current I_1 will flow. When Q1 is cutoff a transient current I_3 will be sinked into $-V_{SS}$ discharging all capacity connected to the node thereby setting the voltage Va at $-V_{SS}$. The salient point here is that a properly ratioed output circuit will function regardless of the load it is driving. In the case of gate arrays, if an error is made in loading an output, the circuit will still operate at a reduced clock rate. This is a vital consideration when doing device check out (DCO) wafer probing on a new circuit design.

4.6.3 Selected Gate Type

Whenever mask programming is involved in such structures as gate arrays a general reduction in circuit response is unavoidable. This is associated with the unknown logic function being implemented, the physical separation of elements and the loading requirements placed on the circuit. Since buffered FET logic has the highest operational speed of the gate types available and other qualities as outlined in Section 4.7.2, it has been selected as the gate type to be used in this program.

4.7 SPICE/TRACAP Comparative Analysis

A repeat of the analysis performed in Section 4.5 was carried out using a MESFET model (Modified JFET), embedded in the REDAC, (Rockwell Electronic Design Analysis Codes), program used in the Anaheim circuit design community. REDAC consists of a component data bank and four integrated programs. Of the four programs, TRACAP (Transient Circuit Analysis Program), a time history or time domain analysis program provides circuit transient response to stimuli such as noise, radiations, voltage, state changes, etc.

Table X compares the analytical results derived from analysis performed using the SPICE and TRACAP programs and Figure 4.13 dispalys the power-delay product versus the various loading conditions. The results track reasonably well except in the area of output voltage swing where the TRACAP analysis indicates a fixed output swing which is independent of the loading. This anomaly will be reviewed with Rockwell CAA/CAD personnel to determine what steps if any will be required to adjust REDAC model parameters since this model will be used for all future circuit analysis.

TABLE X.

COMPARISON OF SPICE AND TRACAP ANALYTICAL RESULTS
OF THE 3 STAGES FET LOGIC (FL) RING OSCILLATOR

CIRCUIT LOADING		GATE PROPAGATION DELAY (Ps)		POWER DISSIPATION/GATE (MW)		(POWER)-(Delay) (fτ)		Output Amplitude (Volts)	
FAN OUT	CAP. LOADING (fF)	SPICE	TRACAP	SPICE	TRACAP	SPICE	TRACAP	SPICE	TRACAP
1	20	153	137	1.8	1.7	275	233	1.1	1.6
2	20	193	158	1.8	1.7	347	269	1.0	1.6
3	20	233	180	1.8	1.7	419	306	0.9	1.6
1	50	215	222	1.8	1.7	311	377	1.1	1.6
2	50	258	244	1.8	1.7	396	415	1.0	1.6
3	50	303	265	1.8	1.7	459	451	0.9	1.6
1	100	323	366	1.8	1.7	455	622	1.1	1.6
2	100	368	381	1.8	1.7	576	648	1.0	1.6
3	100	438	400	1.8	1.7	648	680	0.9	1.6

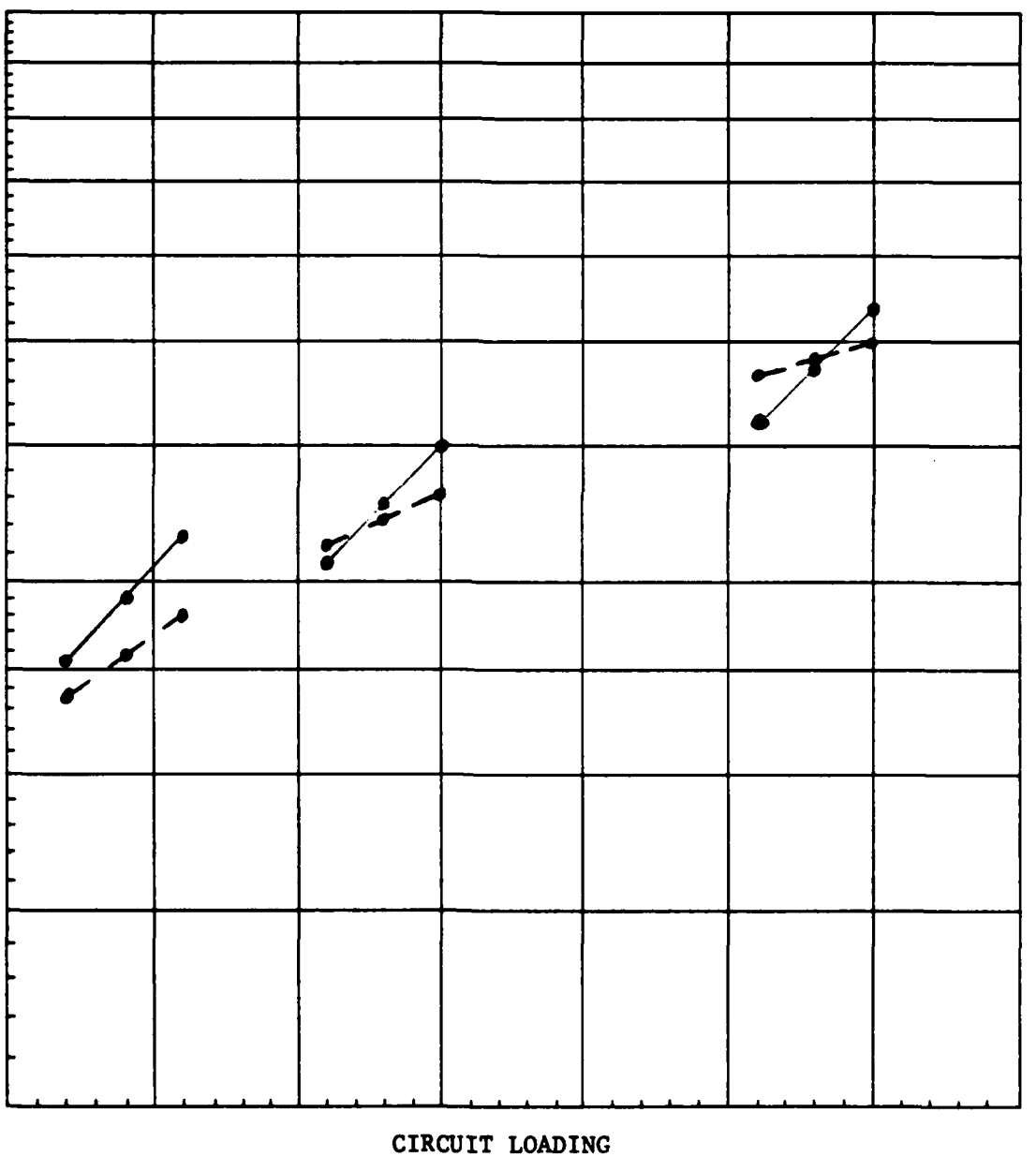


Figure 4.13 Comparison of Power-Delay Products based on SPICE AND TRACAP Analysis

4.8 D Type Flip-Flop Design and Analysis

One of the elements to be used in the storage logic array (SLA) is a D type flip-flop structured from 3-input NOR gates as shown in Figure 5.5. Using custom design this device will be optimized for speed, area efficiency and minimum power requirements.

4.8.1 D Flip-Flop Design

The NOR-gate used to implement the D flip-flop is shown in Figure 4.14 along with the transistor widths and diode dimensions. The same dimensions were used for all gates regardless of their location within the flip-flop. Although this will not yield the most optimized design, we can determine basic speed and input pulse sensitivities of the flip-flop.

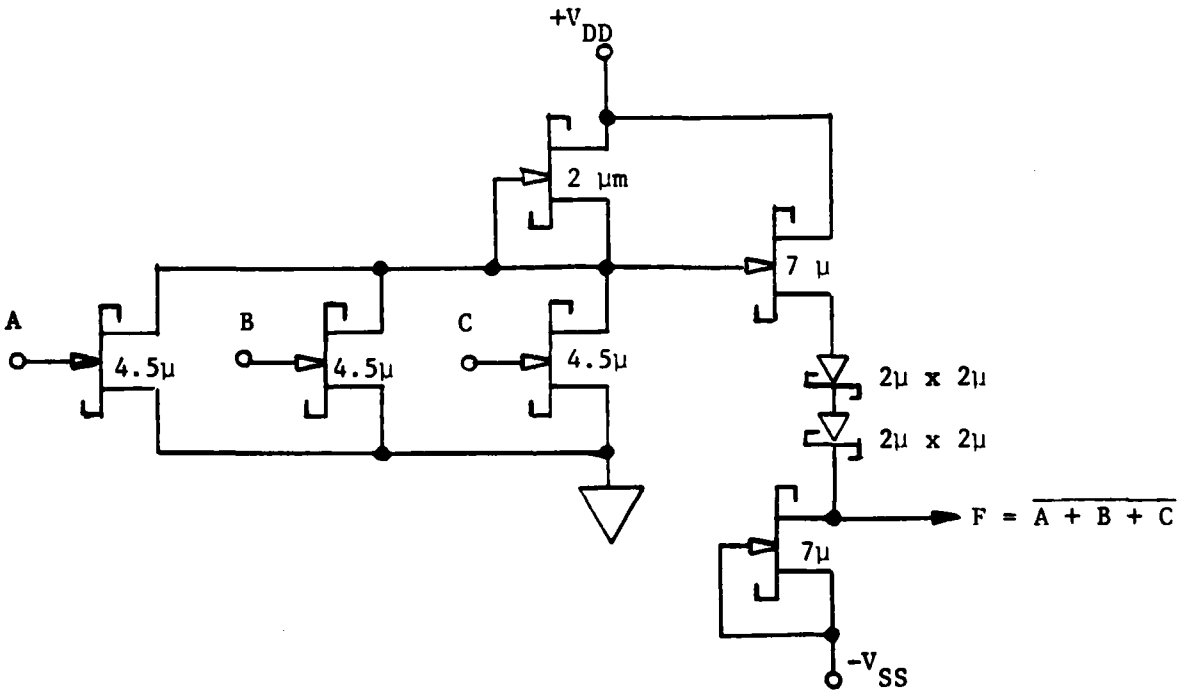


Figure 4.14 3-Input NOR gate used in SLA D Flip-Flop

4.8.2 D Flip-Flop Analysis

For analytical purposes the flip-flop has been modified and connected to perform a divide by 2 function (Figure 4.15). Certain loading was assumed to approximate the expected conditions to be encountered within the SLA .

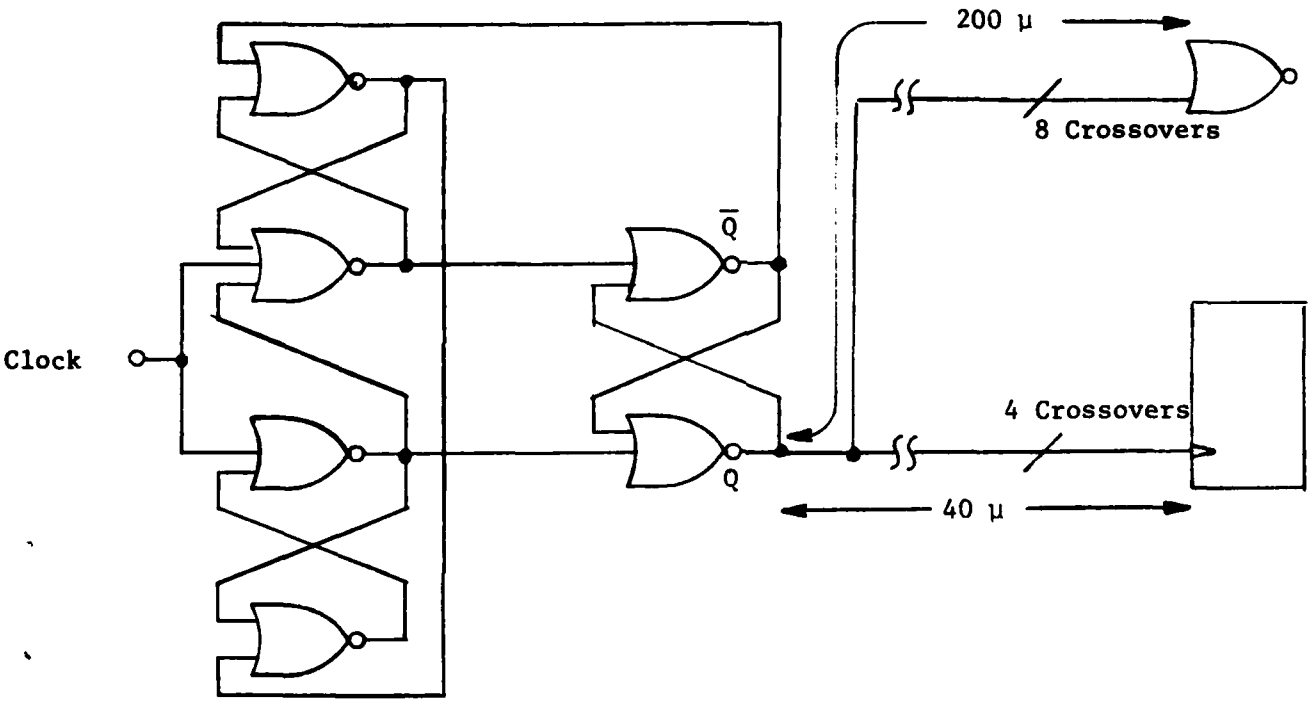
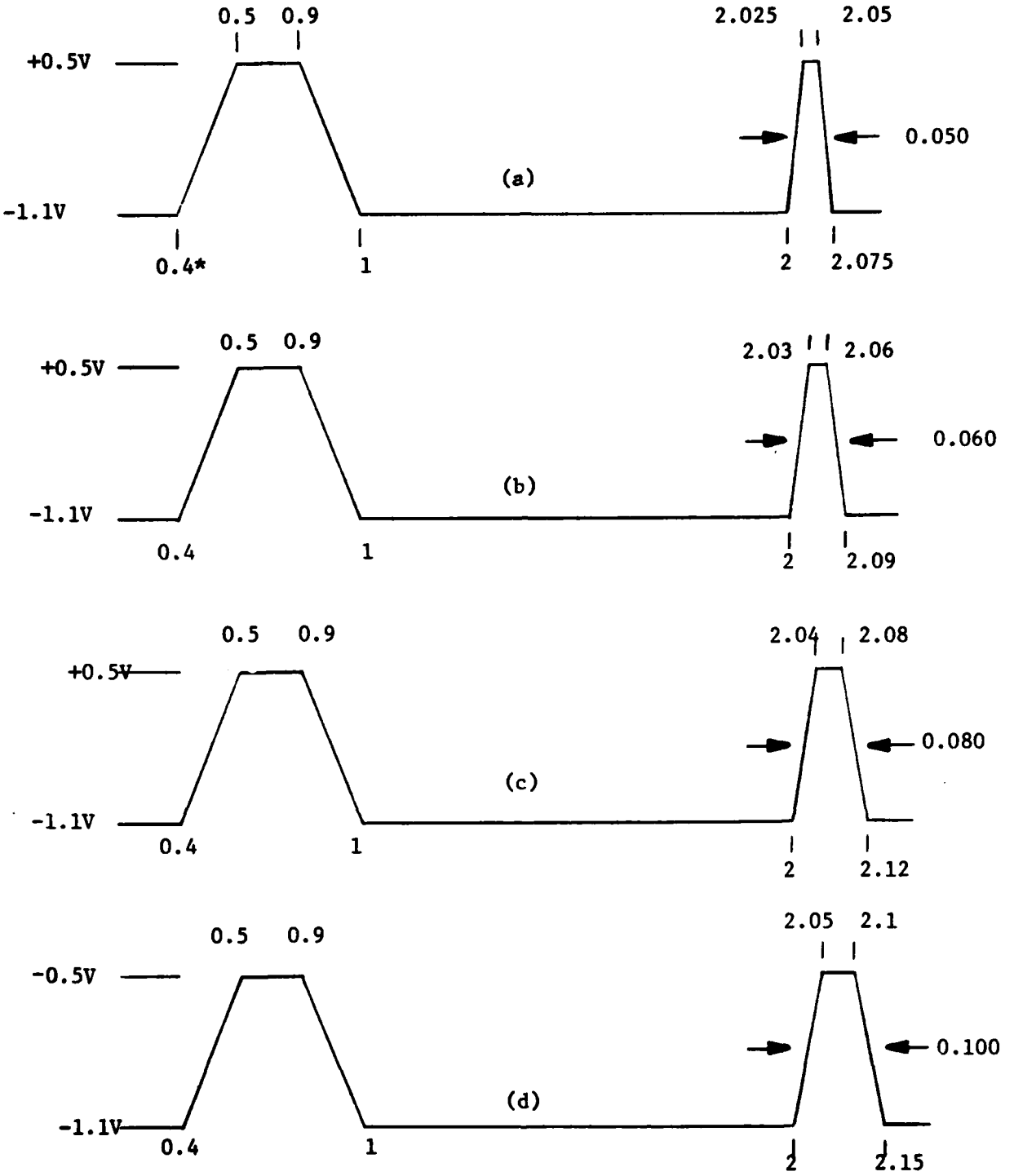


Figure 4.15 D Flip-Flop and Loading Used in Analysis

To determine the sensitivity of the flip-flop to narrow input pulses (clocks). Four test cases were performed using input clocks as shown in Figure 4.16 a, b, c and d. Analysis indicates that a 100 psec pulse width will trigger the flip-flop, however, an 80 psec pulse width or less will not. The maximum operating speed of the flip-flop is 2.5 GHz as shown in the computer plot (Figure 4.17). An increase in operation to 3 GHz can be accomplished by adding another feedback loop from the Q output to the input.



*All time references are in nano seconds.

Figure 4.16 Clock Inputs used in Flip-Flop Sensitivity Analysis

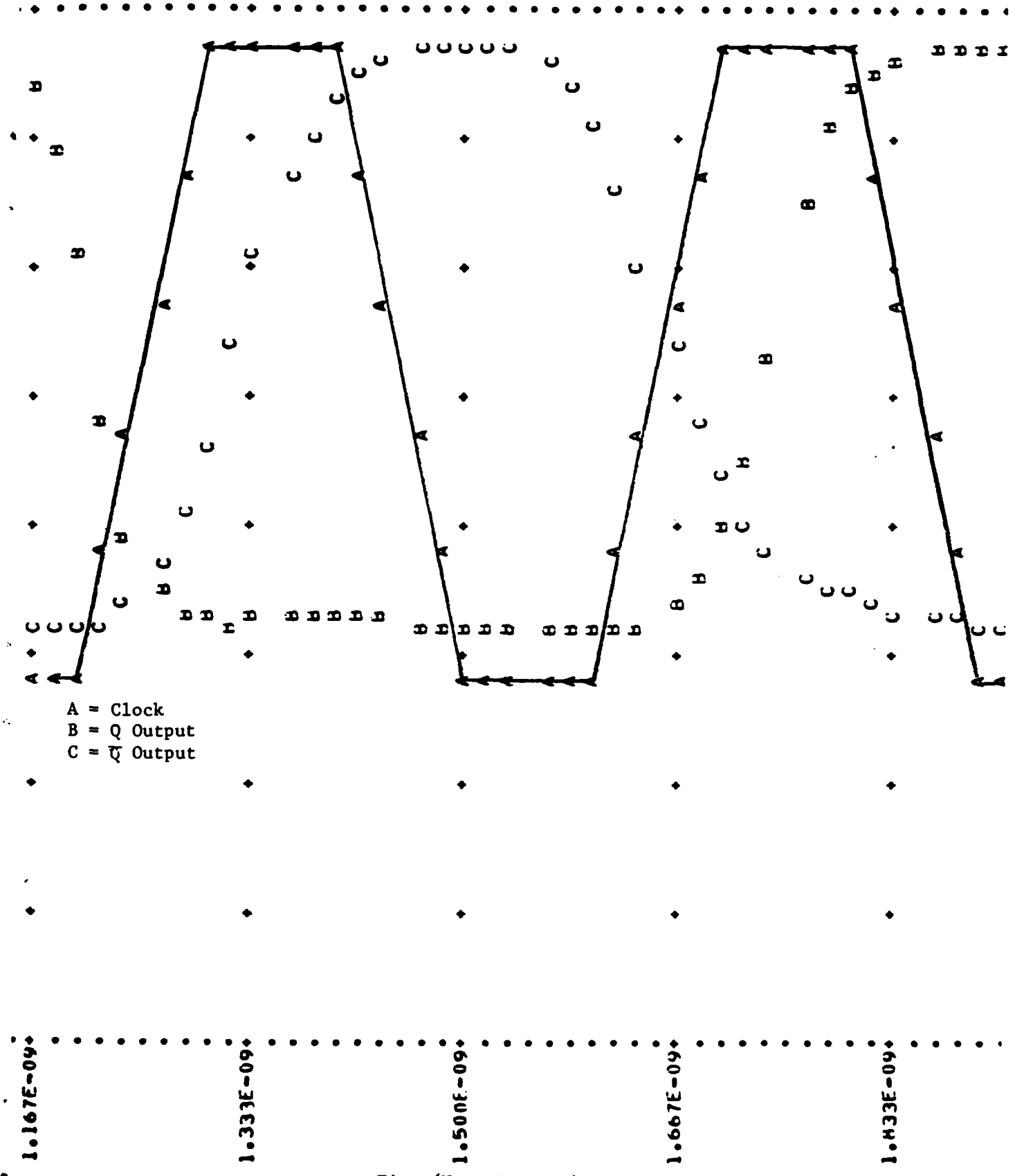


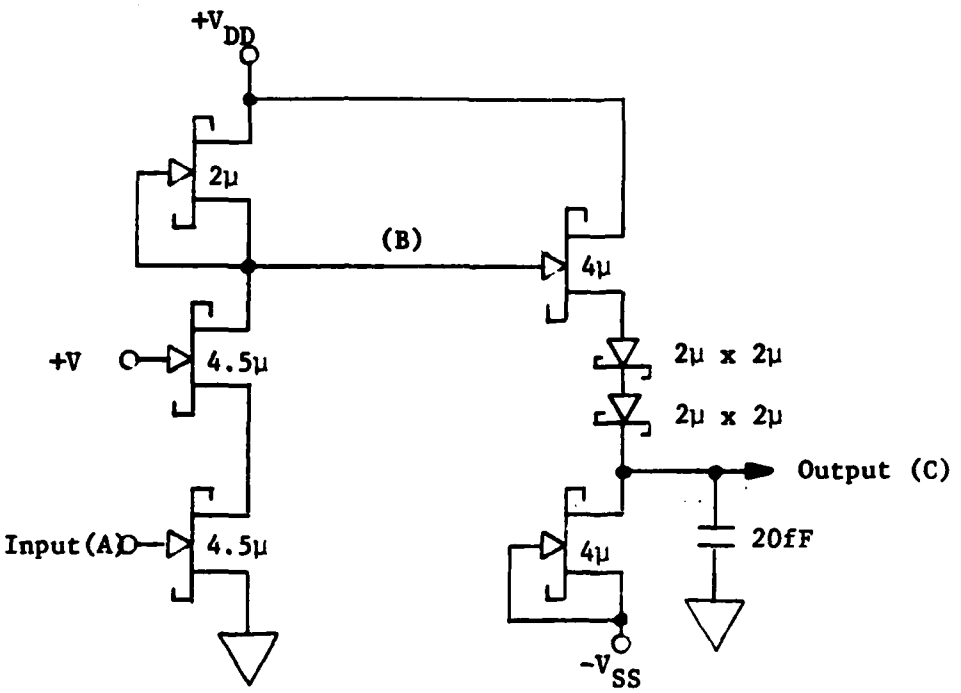
Figure 4.17 Computer Print of maximum Flip-Flop Speed

4.9 NAND Gate Analysis

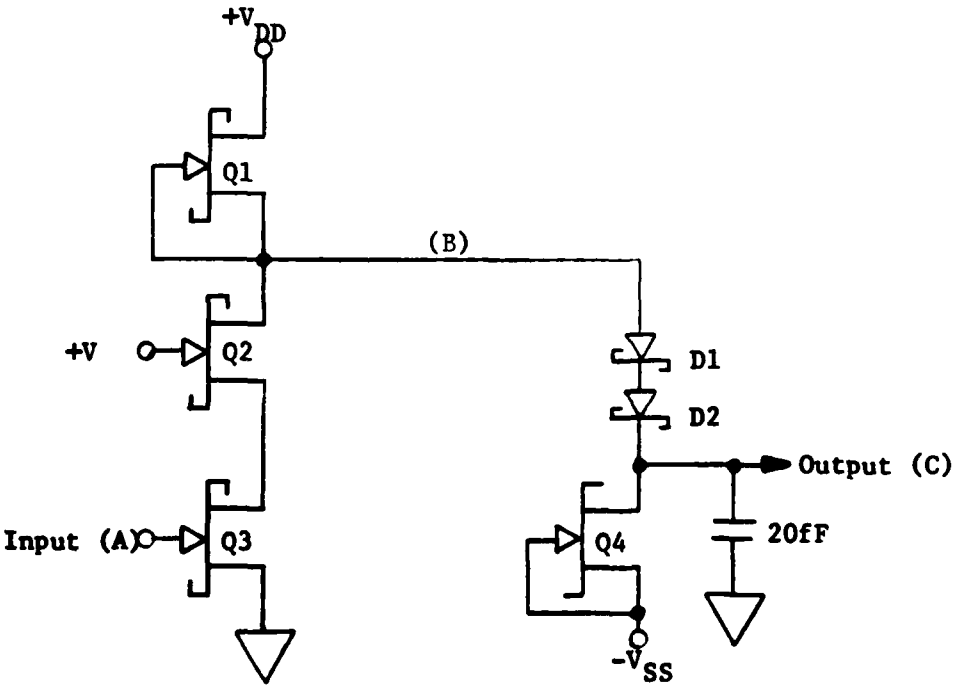
Another basic building block which can be structured from the T/D kernels (Figure 5.6) of the SLA is a 2-Input NAND gate.

Analysis was performed on Buffered FET Logic (BFL) and FET Logic (FL) gates (Figure 4.18) to determine functional characteristics and transistor/diode dimensions required to drive a fixed 20 femto-farad (fF) load. A 2-input NAND gate designed with the transistor/diode dimensions as shown in Figure 4.18 (a) will drive the required load with output signal characteristics as shown in Figure 4.19 (a), where A = Input signal, B = Buffer input signal and C = Output signal. With a positive going input the output signal delay is 150 psec. For a falling input the delay is 170 psec.

Using the same transistor/diode dimensions and removing the buffer transistor (Figure 4.18 (b)), will produce a nonfunctional circuit. Changing the transistor sizes (Q1 = 8μ, Q2 & Q3 = 18μ) will produce a functional circuit with a delay of 100 psec for a positive going input signal and a 340 psec delay for a negative going input signal. The output signal rise time is approximately 500 psec (Figure 4.19 (b)). To increase the rise time of the positive going output signal, pull-up transistor Q1 was replaced with a saturated resistor. Two test cases were analyzed. In the first computer run the saturated resistor width (Q1) was 2μ, Q2 and Q3 = 12μ and Q4 = 3μ. In the second case Q1 = 3μ, Q2 and Q3 = 18μ and Q4 = 4μ. Both runs indicated substantial improvement over the use of a standard trasistor pull-up. The analytical results from run number 1 is shown in Figure 4.19 (c). A delay of 100 psec is indicated for a positive input signal and a 130 psec delay for a negative signal. Basically this analysis shows there is no advantage to using FET logic (FL) over buffered FET logic (BFL) for NAND gate applications.

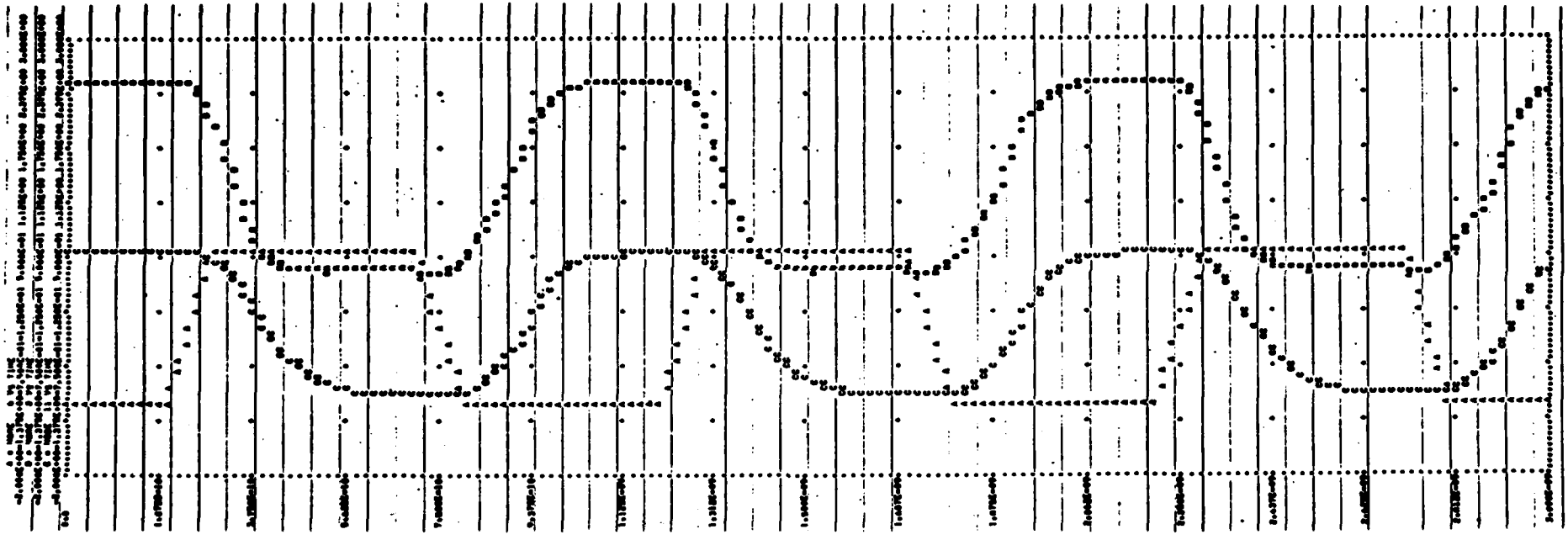


(a) Buffered FET Logic NAND Gate



(b) FET Logic 2-Input NAND Gate

Figure 4.18 BFL and FL 2-Input NAND Gates



Time

Figure 4.19 (a) BFL 2 - Input NAND Gate Analytical Results

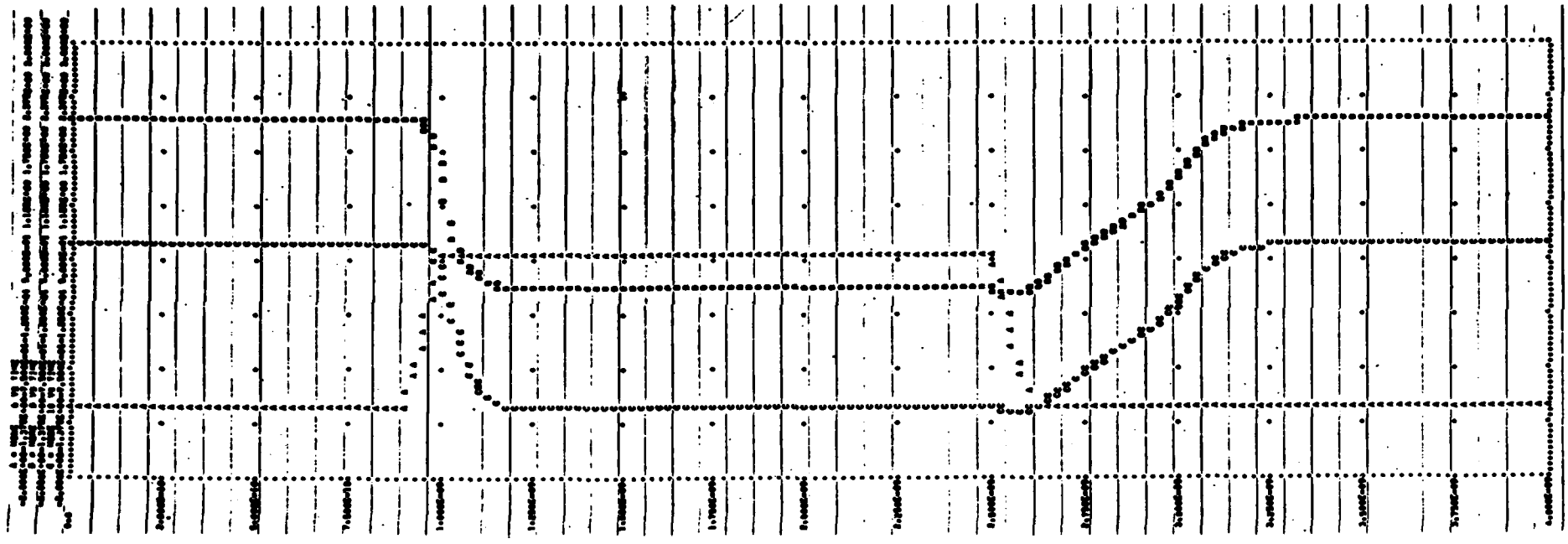


Figure 4.19 (b) FL 2-Input NAND Gate Analytical Results

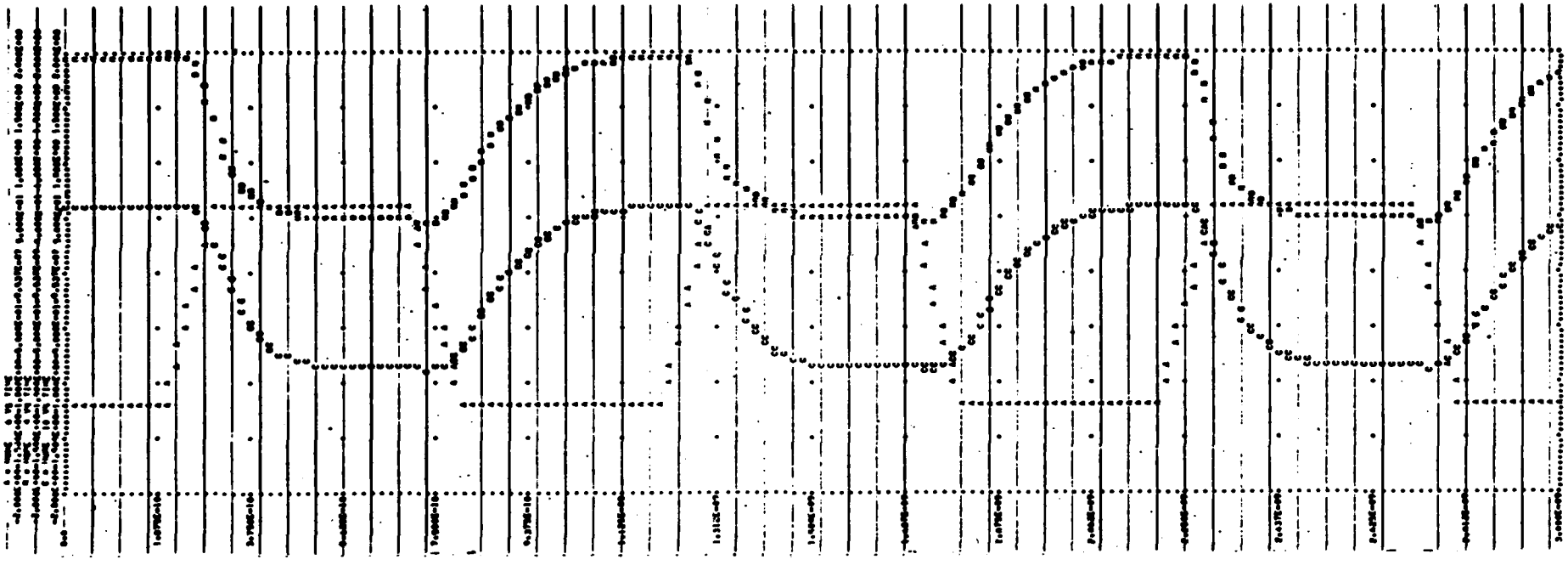


Figure 4.19 (c) FL 2-Input NAND Gate Analytical Results (Saturated Resistor Pull-Up)

5. CHIP DESIGN

5.1 Mask Programmable Function and Logic Array Chip

A preliminary plan of the proposed 6 cell mask programmable function and logic array (MPFLA) chip is shown in Figure 5.1. A cell size of 80 to 100 mils on the side is projected with pad layout, (Figure 5.2), organized to fit the 150 x 150 mil cavity of a 28 pad leadless chip carrier, (400 x 500 mil.) developed by the Biodynamics Research Unit of Mayo Clinic.

5.2 Cell 1 and 2 Floor Plan

As indicated in Figure 5.1, cells 1 and 2 are reserved for the process monitors, yield test structures and modeling structures. A floor plan of these cells based on preliminary estimates of area requirements is shown in Figure 5.3. It is expected that slight modifications to this plan will develop as details of total processing, yield and modeling requirements are finalized.

5.3 Storage Logic Array

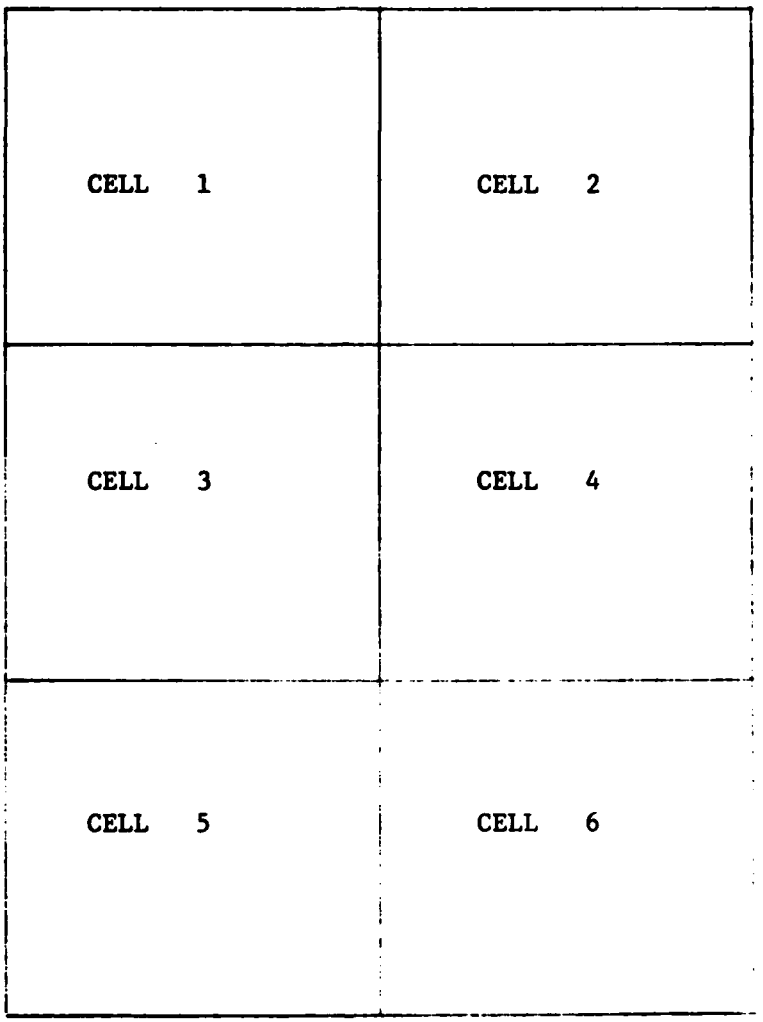
Cells 3, 4 and 6 will be used to implement mask programmable functions based on the storage/logic array (SLA) module shown in Figure 5.4. The backbone of the SLA approach is a customized D-type flip-flop, (Figure 5.5), surrounded by un-committed transistor/Diode (T/D) kernels (Figure 5.6). Some basic logic functions which can be implemented with the T/D kernels is shown in Figure 5.7. Details on the physical layouts of the flip-flops and T/D kernels for ease of personalizing the SLA has not been worked out in detail, however, an optimal solution would be a layout requiring one mask (2nd level metal) interconnect.

Other alternatives may require a two mask change (VIA and 2nd level metal) or a 3 mask change (1st metal, VIA and 2nd level metal).

5.4 Cell 3 Circuit Functions

Circuit functions to be implemented in the SLA/s of cell 3 include a divide by 6/7, divide by 10/11, 4-bit down counter with synchronous load and asynchronous clear and a phase detector.

A logic diagram of the ÷ 6/7 and ÷ 10/11 is shown in Figure 5.8. The basic function of these devices is for speed/power comparison of custom circuits contained in cell 5. The 4-bit down counter (Figure 5.9)and the phase detector (Figure 5.10)are system functional elements to be implemented as required for compliance with the kit parts list.



CELL 1, 2 - Process Monitors, Yield and Modeling Structures

CELL 3 - Storage Logic Array Configured as Prescalers, Down Counter and Phase Detector

CELL 4 - Storage Logic Array Direct Digital Frequency Synthesizer Elements

CELL 5 - Mask Programmable Prescalers

CELL 6 - Pseudo Random Sequence Generators

Figure 5.1 - Mask Programmable Function and Logic Array (MPFLA) Chip

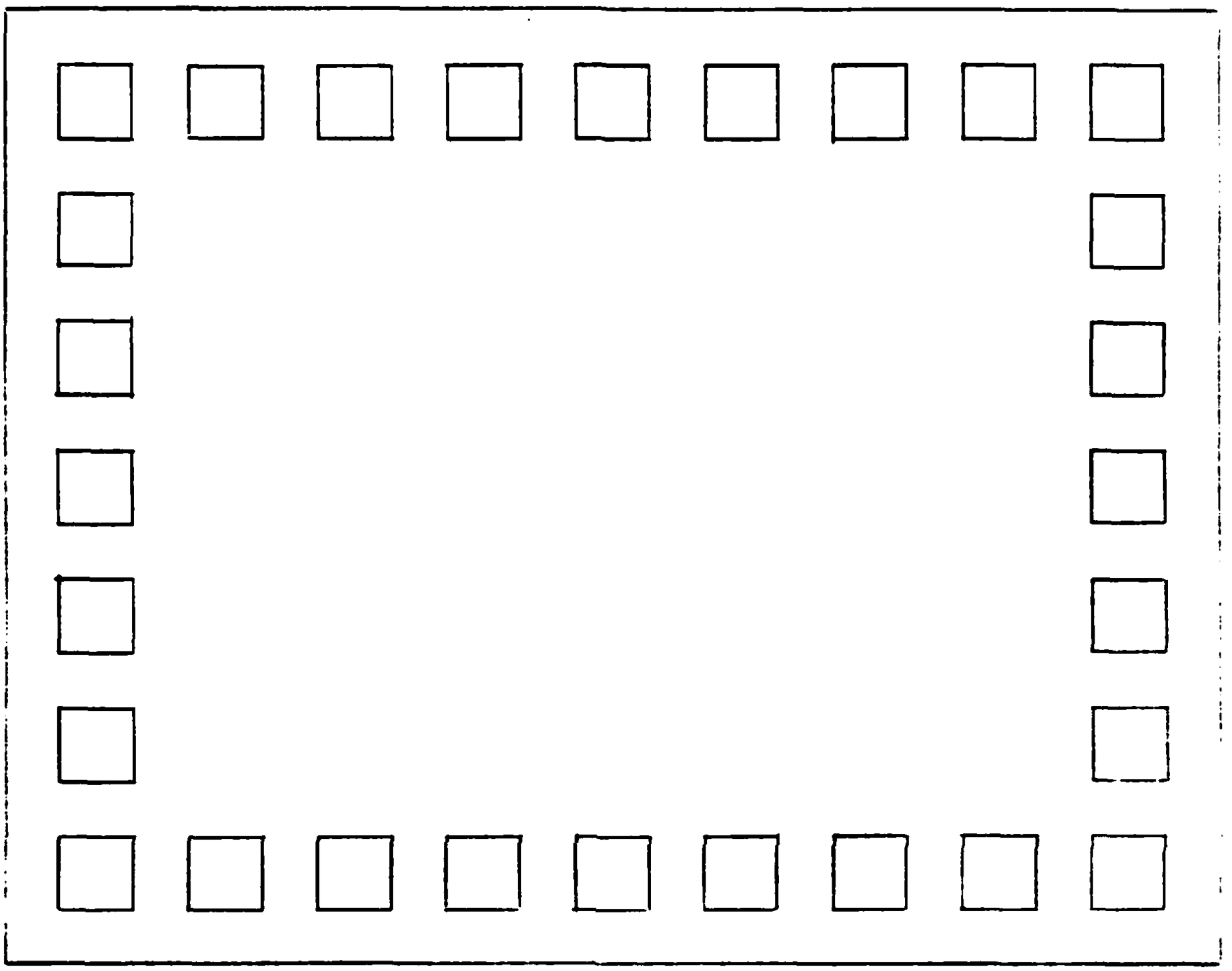
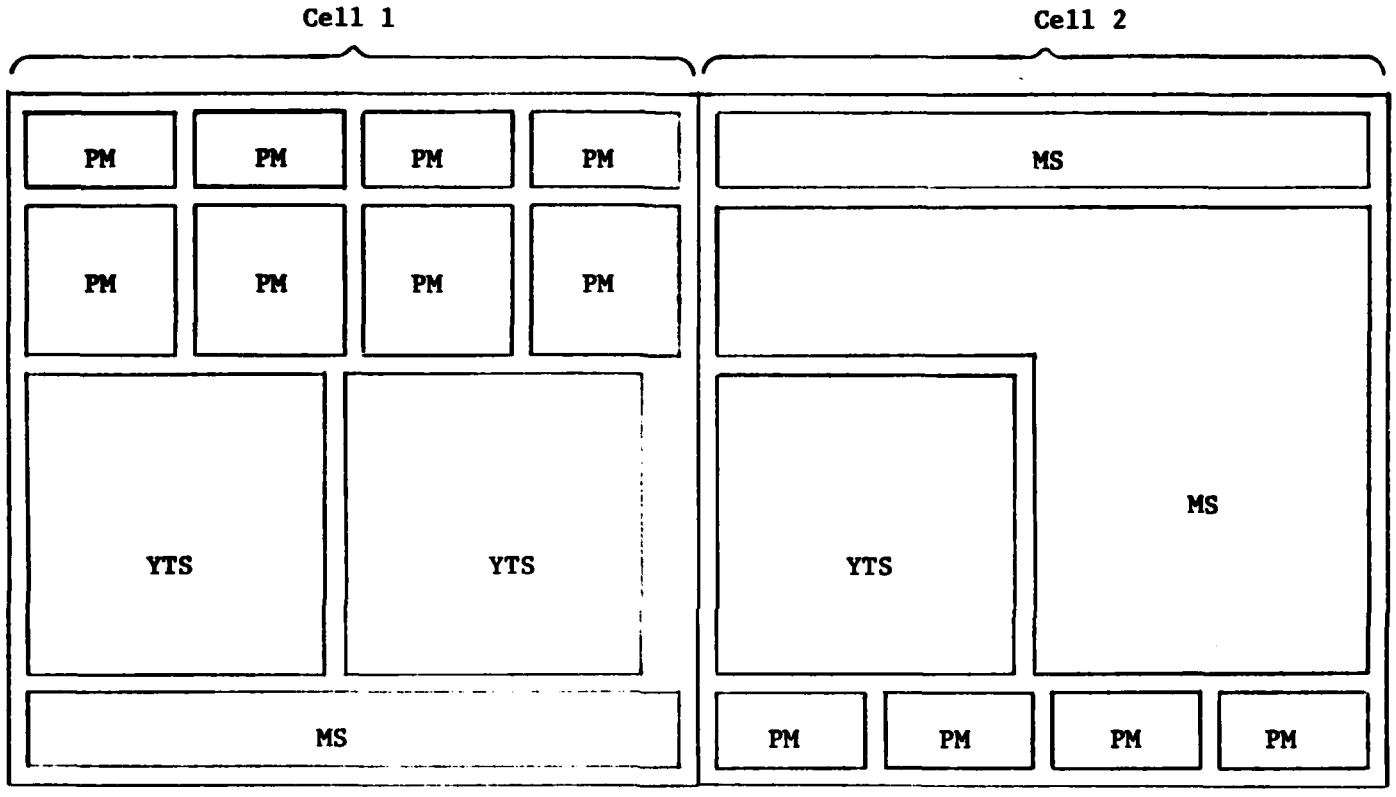


Figure 5.2. Pad Configuration of Cell to Match 28 Pad Leadless Chip Carrier



PM - Process Monitor

YTS - Yield Test Structure

MS - Modeling Structure

Figure 5.3. Tentative Floor Plan for Cells 1 and 2.

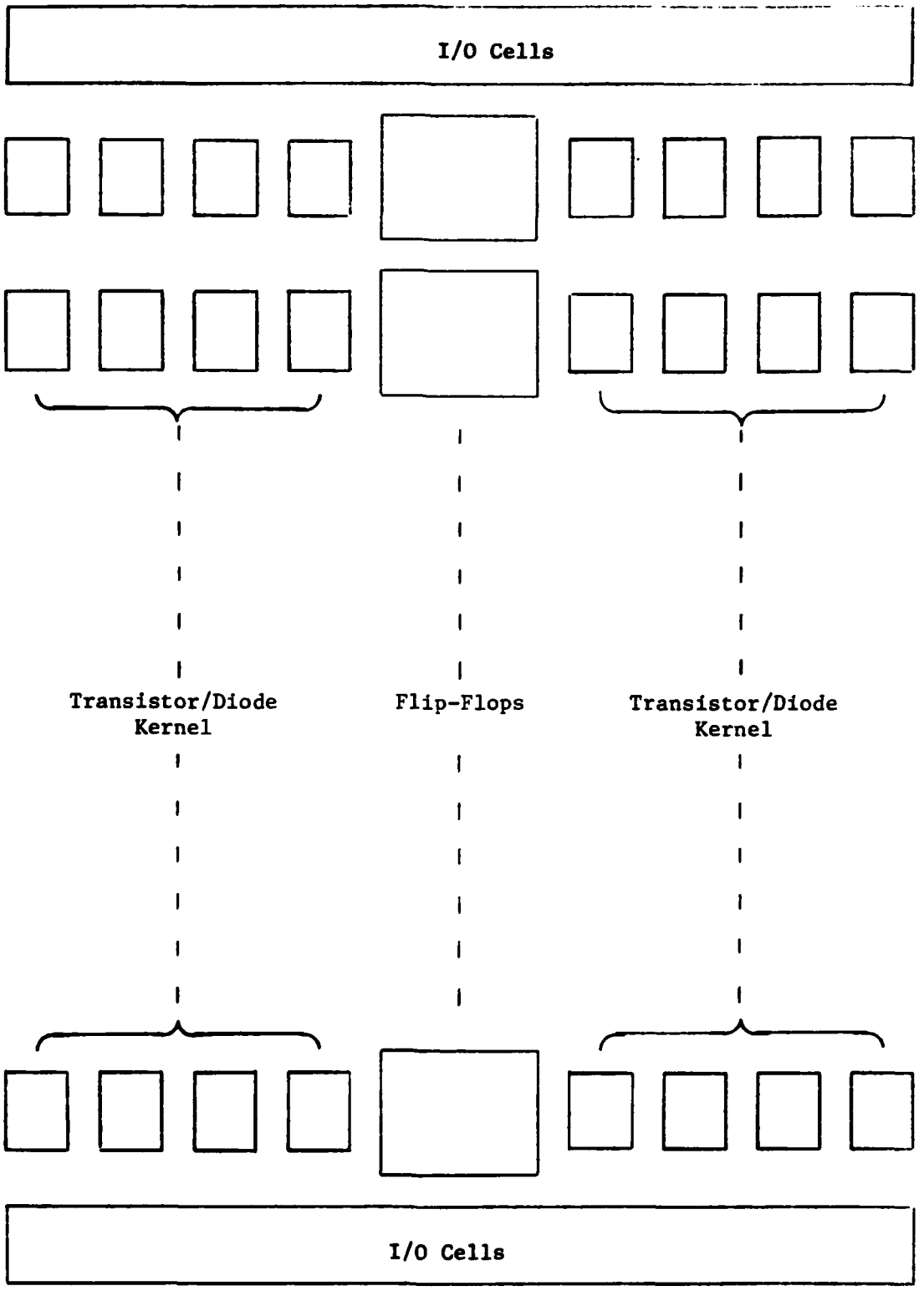
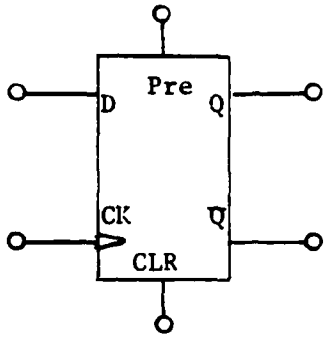


Figure 5.4 Storage/Logic Array (SLA) Module Block Diagram



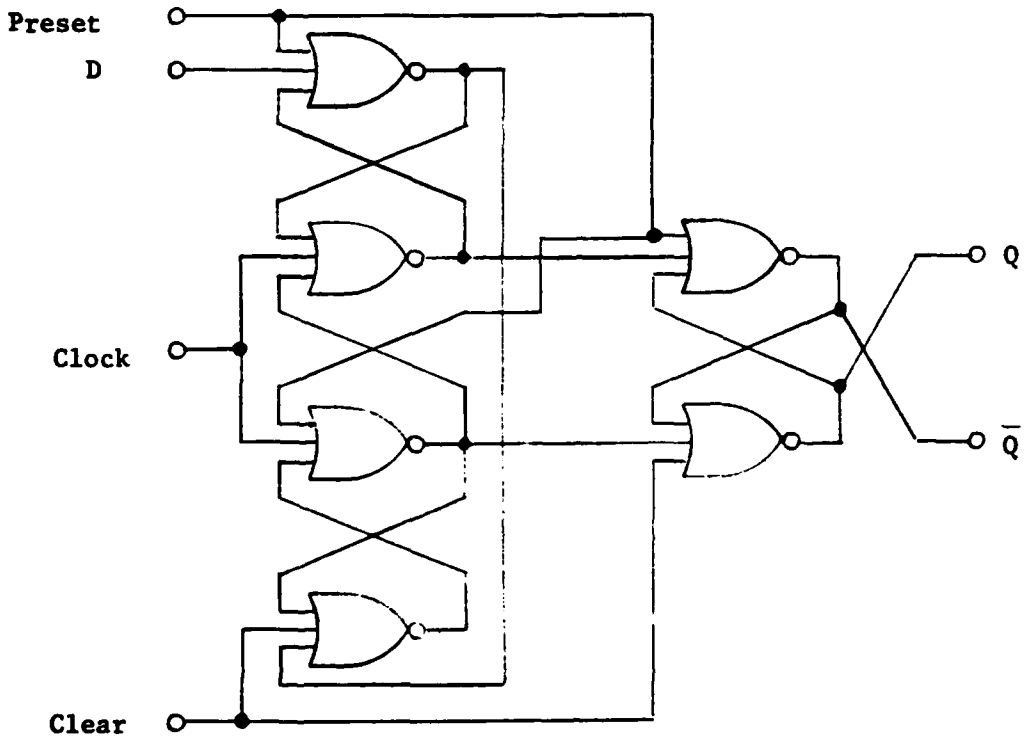


Figure 5.5 Custom D Flip-Flop used in SLA

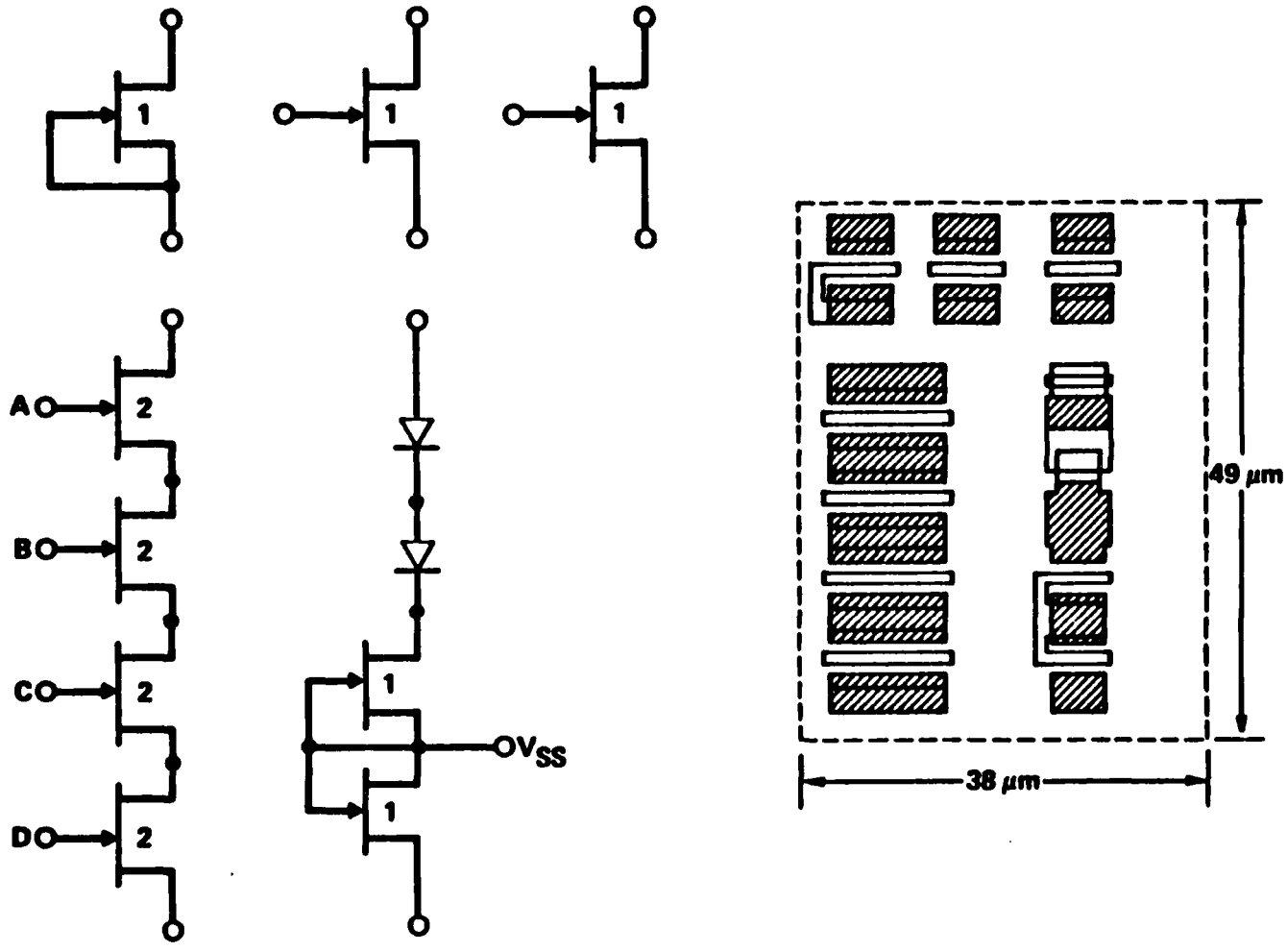
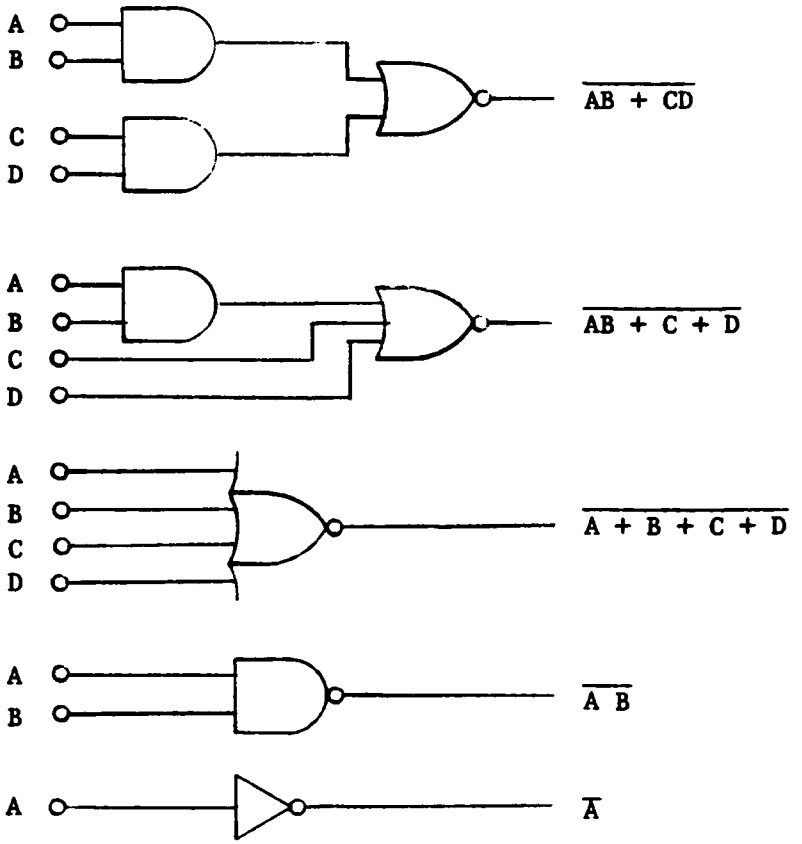
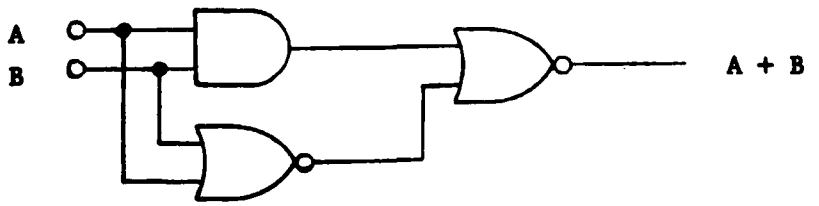


Figure 5.6 Proposed Transistor/Diode Kernel

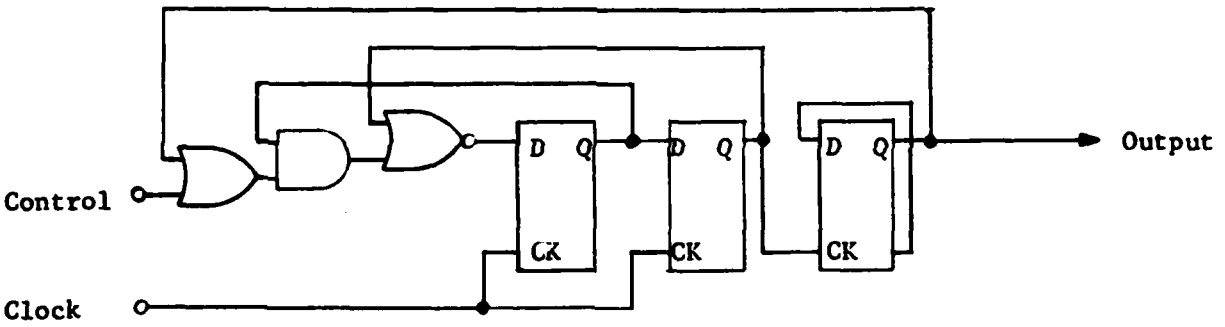


(a) Basic Functions Created with a Single T/D Kernel

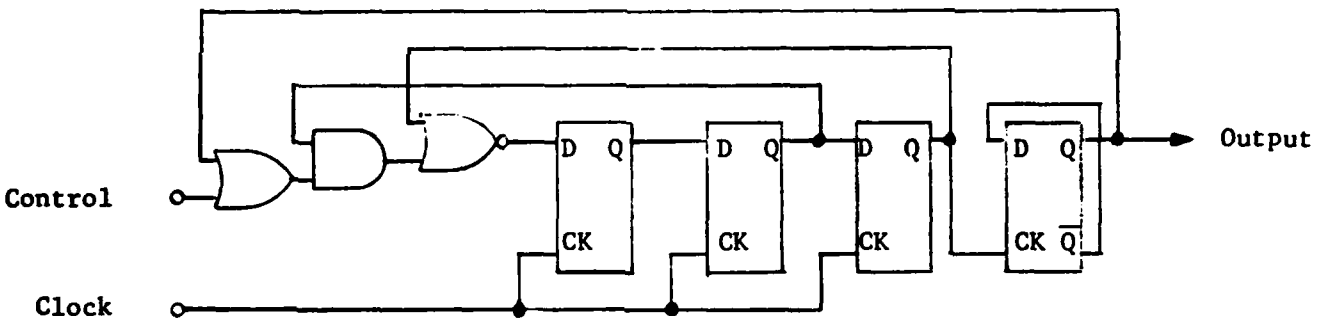


(b) Basic Function Generated with 2 T/D Kernel

Figure 5.7 Basic Logic Functions Implemented with Transistor/Diode Kernels



(a) Divide by 6/7



(b) Divide by 10/11

Figure 5.8 SLA Prescaler Design

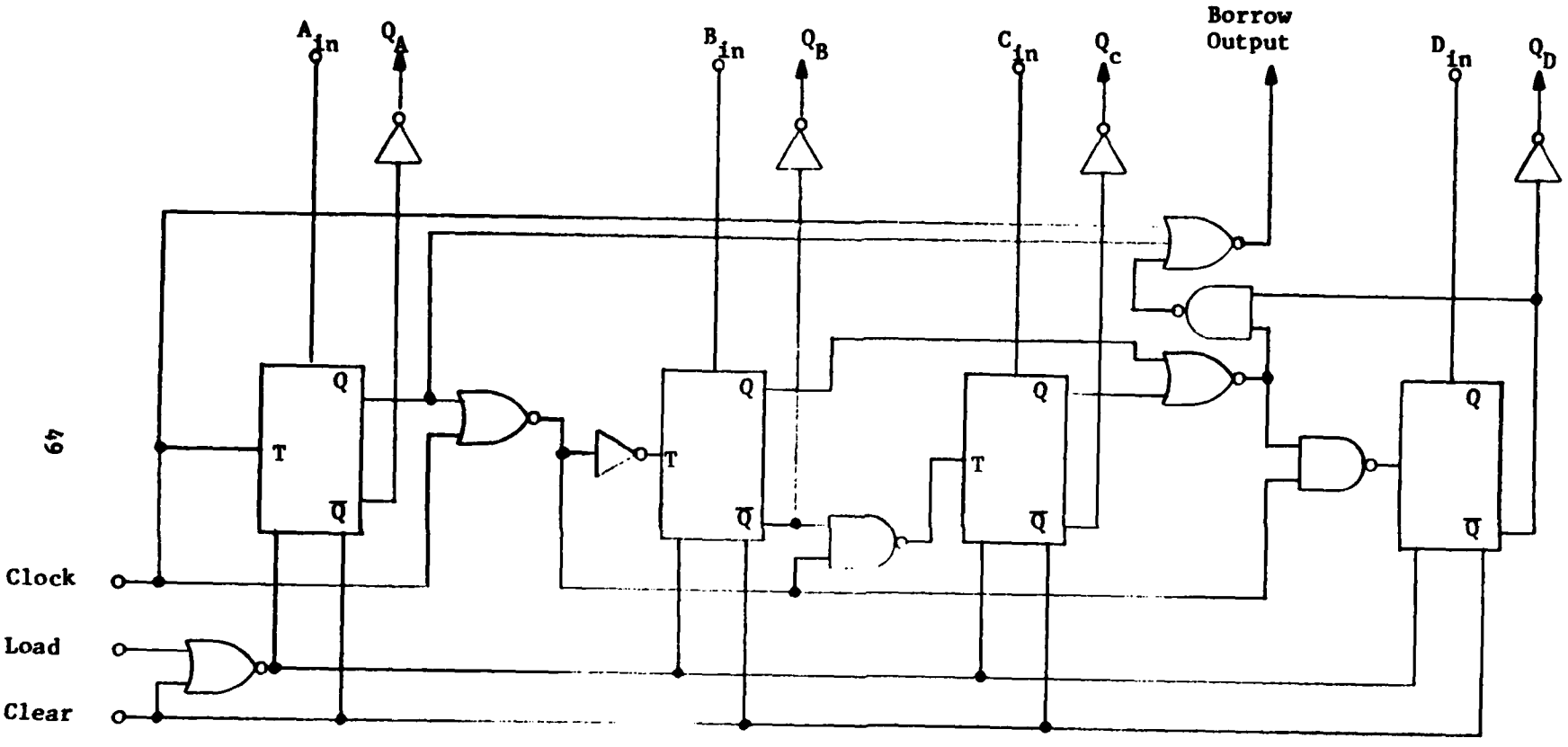


Figure 5.9. Synchronous 4-Bit Down Counter with Synchronous Load and Asynchronous Clear

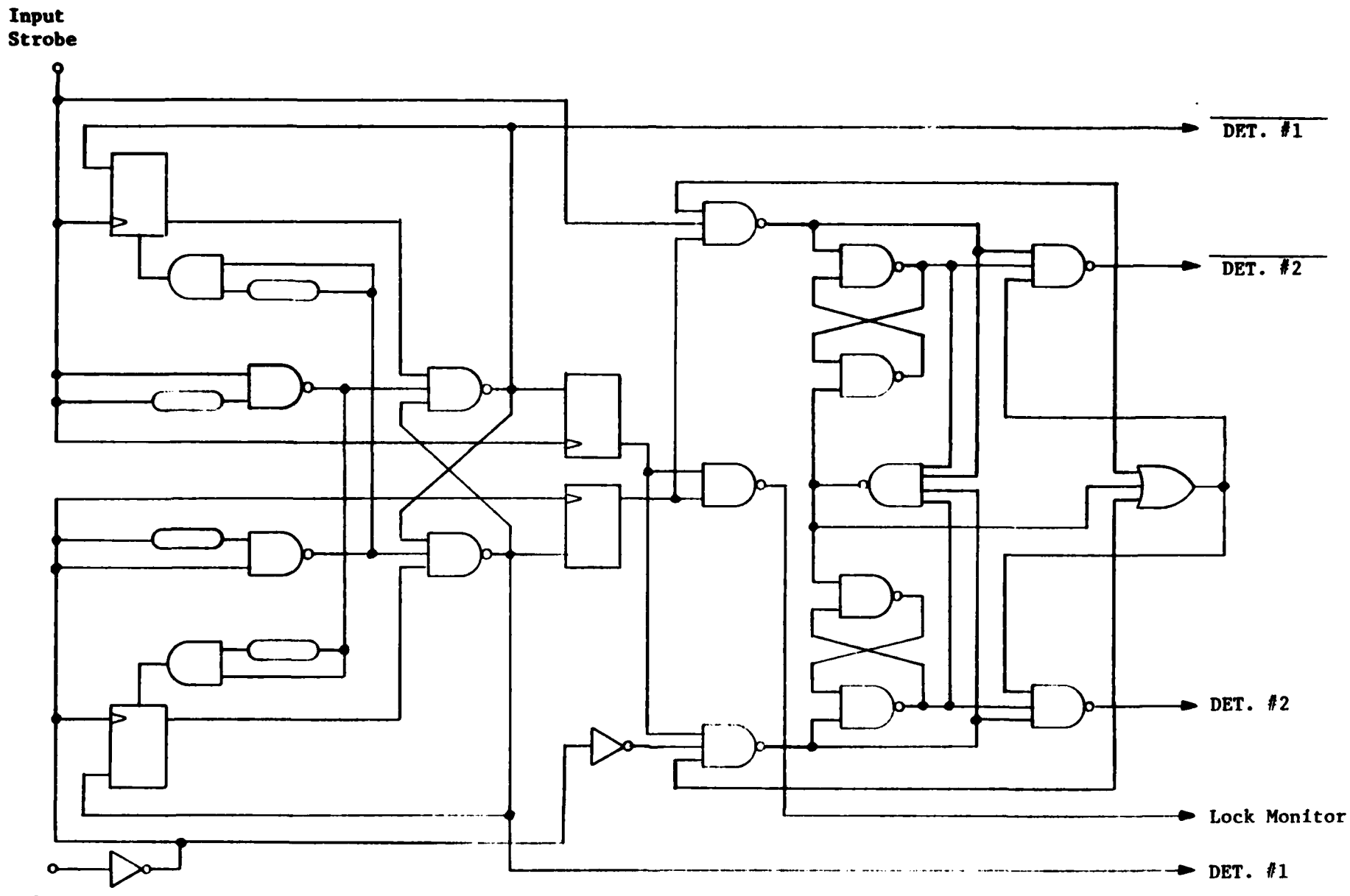


Figure 5.10 Logic Diagram - Phase Detector

The 4-Bit down counter (Figure 5.9) will demonstrate the speed/power capabilities of a basic circuit function required as a frequency control element in an indirect frequency synthesizer. Likewise, the phase detector (Figure 5.10)which is a building block of a complete phase-lock-loop (Figure 2.1) will demonstrate the operational characteristics of a type I and II phase detector and lock monitor circuit.

5.5 Cell 4 Direct Digital Frequency Synthesizer Functions

Cell 4 is composed of two storage/logic array modules which have been committed to the implementation of a 4-bit accumulator and shift register as required for the development of a direct digital frequency synthesizer.

5.6 Cell 5 Prescalers

A quadruplet of mask programmable prescalers will be placed into Cell 5. A custom design (Figure 5.11) will be used as the basic element and will be personalized using the 2nd level metal interconnect. Figures 5.12 thru 5.15, show the connections required to implement divide ratios of 6/7, 10/11, 20/21 and 40/41. An alternate approach would require only one basic element and four 2nd level metal mask layers. This would increase cost for additional mask and increase the number of wafers to be processed and the time required for processing. To maintain the program within the time/cost constraints the alternate approach will not be implemented.

5.7 Cell 6 Pseudo Random Sequence Generators

The pseudo random sequence generator (Figure 5.16) will be structured in Cell 6. Two designs will be contained within the cell. One will be a custom layout and the other will be implemented using the SLA module. With a 12 stage shift register a maximal length sequence of $2^{12}-1$ bits will be generated. Incorporating feedback taps as specified, the generated polynomial is: $G(X) = x^{12} + x^{11} + x^{8} + x^{6} + 1$.

The maximum operating speed of the circuit will be limited by the exclusive - OR circuits in the feedback network. One technique of eliminating the slow feedback is to implement the circuit with exclusive-OR elements in a feed forward path and extend the shift register length to compensate for these series elements.

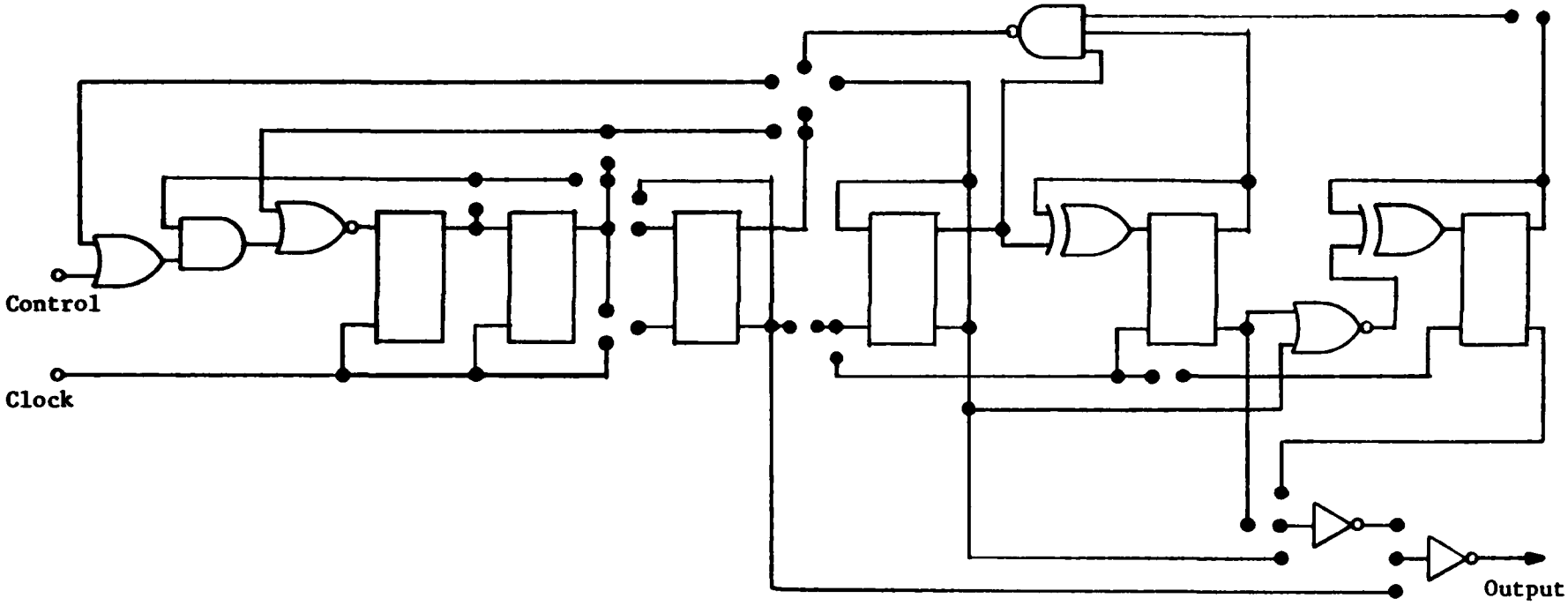


Figure 5.11 Mask Programmable Function (Prescaler)

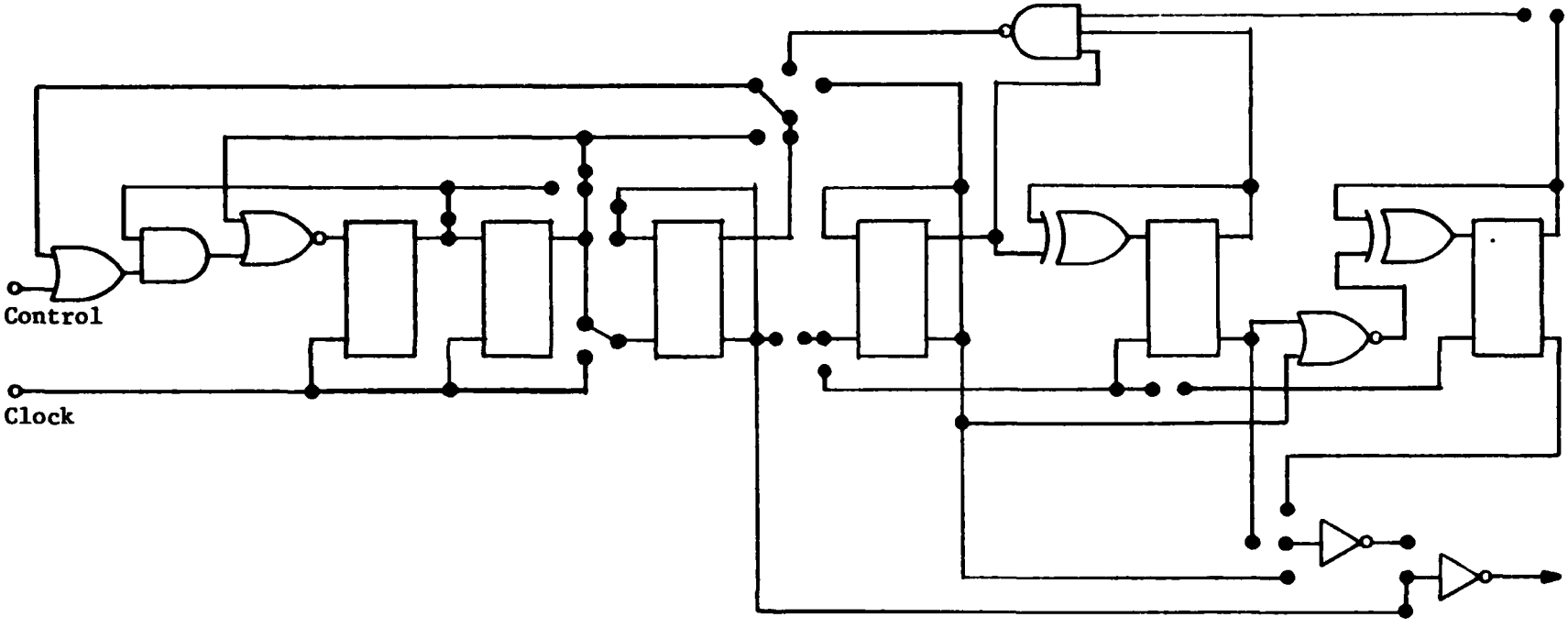


Figure 5.12 Divide By 6/7

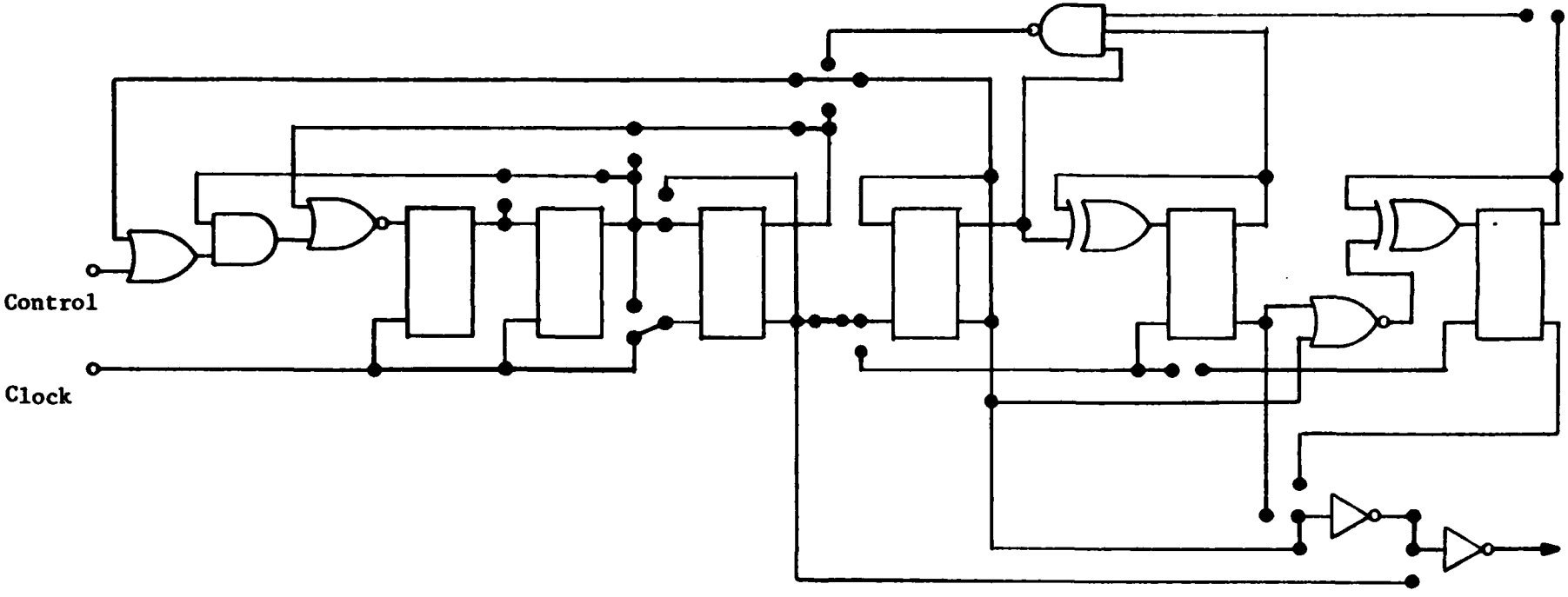


Figure 5.13 Divide By 10/11

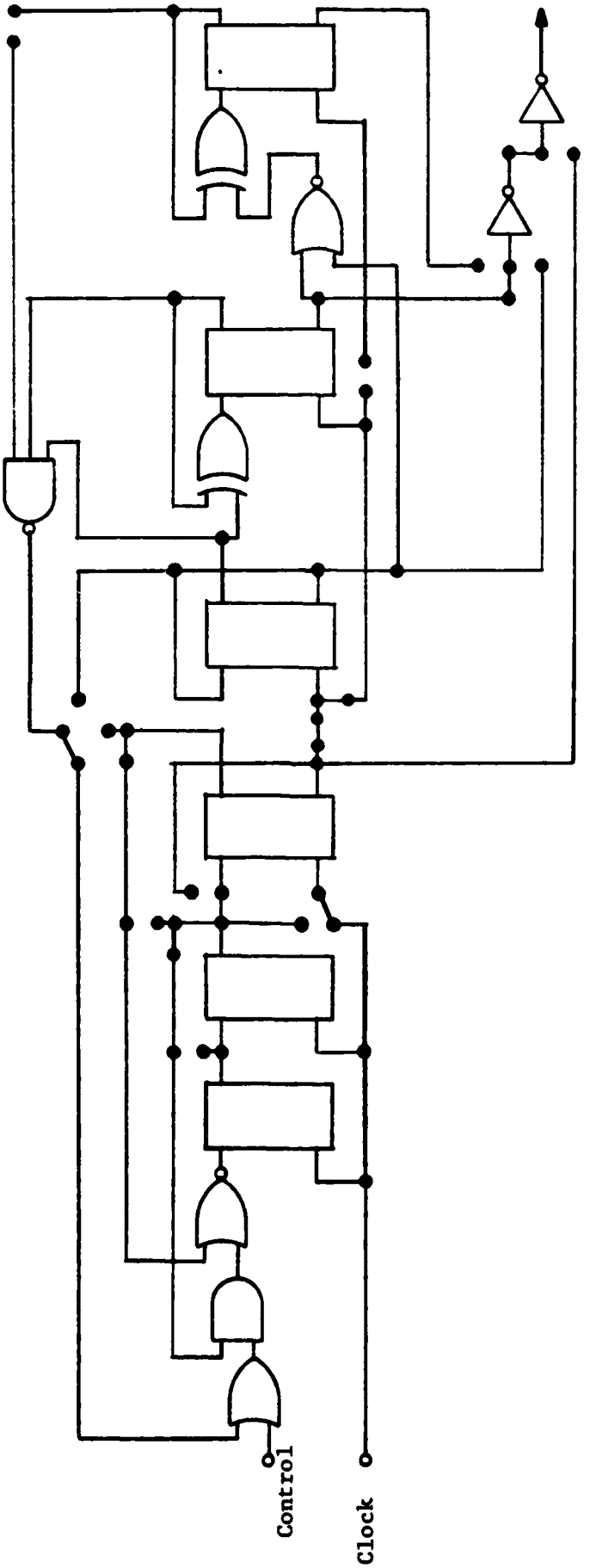


Figure 5.14 Divide By 20/21

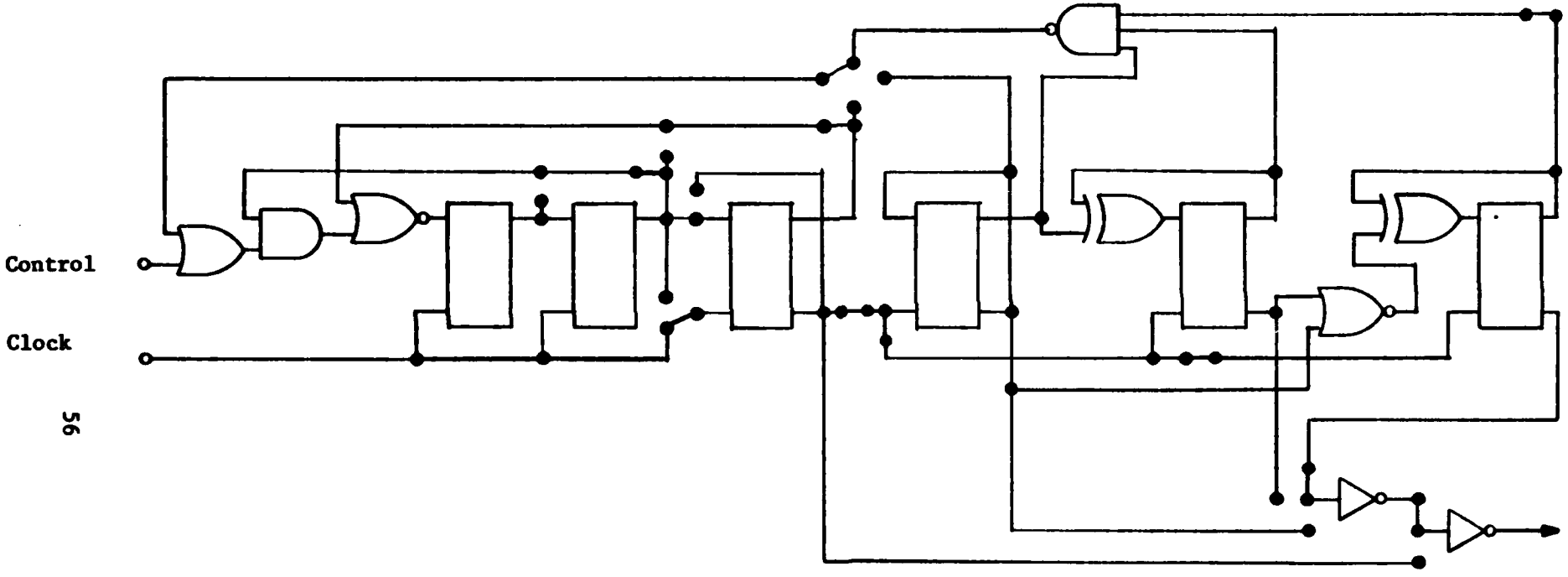
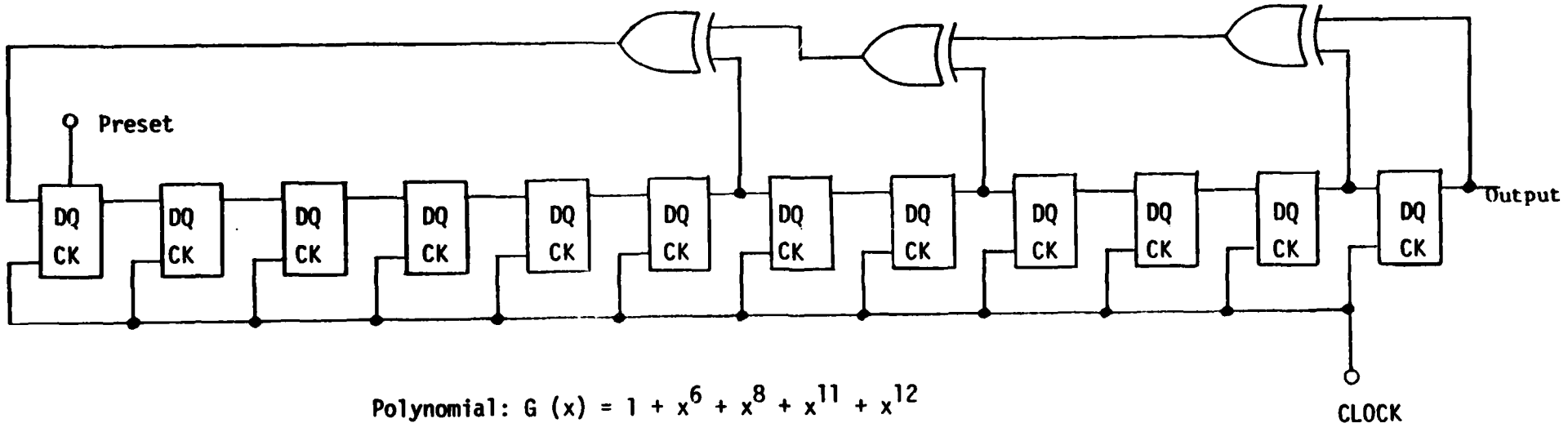


Figure 5.15 Divide by 40/41



Polynomial: $G(x) = 1 + x^6 + x^8 + x^{11} + x^{12}$

Figure 5.16 Pseudo Random Sequence Generator

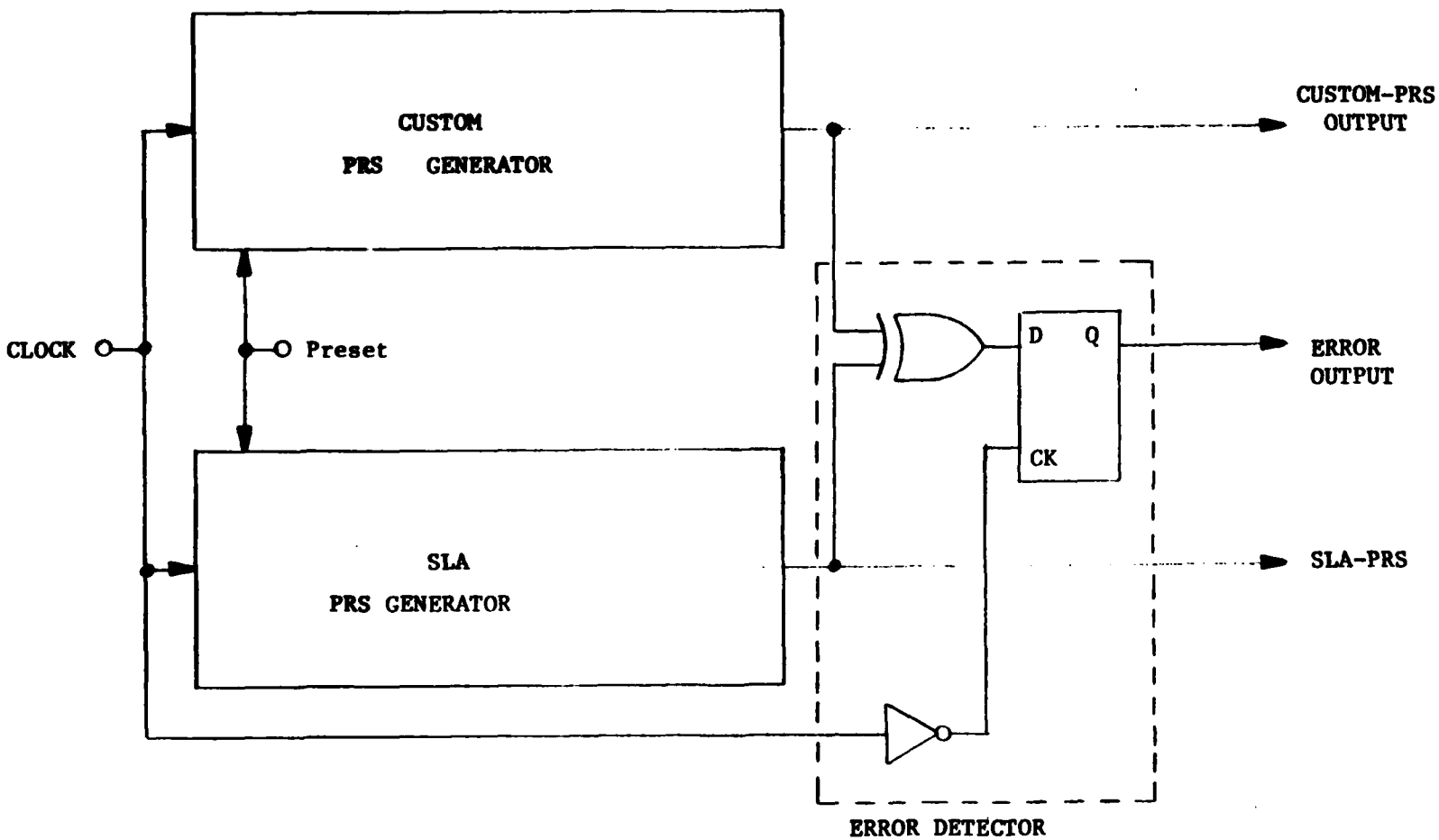


Figure 5.17 Pseudo Random Sequence Generator Error Detector

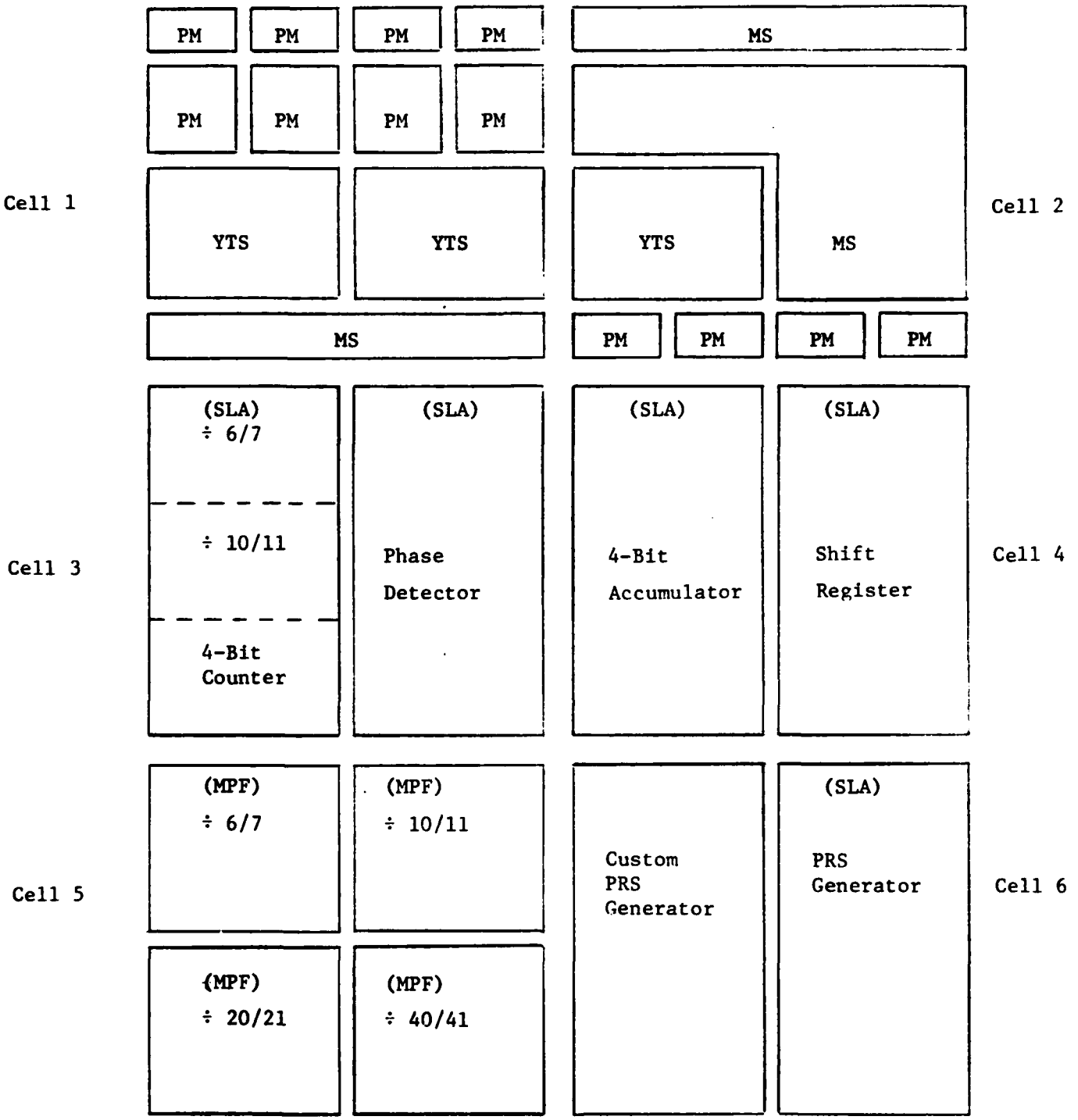
For this program we will use the feedback method to determine the penalties associated with that approach. The addition of a simple circuit (Figure 5.17) will enhance testing as it can be used as an error detector for comparing operation of the two PRS generators. A preset input is included in the design to synchronize the two generators and to eliminate the all "0" illegal state.

5.8 MPFLA Floor Plan

A floor plan of the MPFLA chip is shown in Figure 5.18. Although the drawing is not to scale it does represent accurate chip organization and space allocation.

5.9 Processing Mask Set

A standard 10 layer mask set will be manufactured, as listed in Table XI, for wafer processing which will be performed using the direct implant technique previously developed for implementation of Schottky Diode FET Logic (SDFL) digital circuits



PM = Process Monitors
YTS = Yield Test Structures
MS = Modeling Structures
SLA = Storage/Logic Array
MPF = Mask Programmable Function
PRS = Pseudo Random Sequence

Figure 5.18 Floor Plan of Mask Programmable Function and Logic Array Chip (Not to scale)

TABLE XI

GaAs MASK SET

LAYER #	FUNCTION	POLARITY
1	Alignment Marks	Neg.
2	N^- Implant	Neg.
3	N^+ Implant	Neg.
4	Proton Implant	Neg.
5	Ohmic Contact	Neg.
6	Schottky Metal	Neg.
7	VIA	Neg.
9	2nd Level Metal	Pos
10	Bonding Pads	Neg.
11	Kerf Line	Neg.

6. SYMCAD STUDY

6.1 SYMCAD DESIGN METHODOLOGY

SYMCAD is an interactive symbolic design methodology that is primarily aimed at standard cell, macrocell, and module level VLSI/VHSIC design. The designer uses a very simple interactive procedure to compose a symbolic representation of the circuit topology being implemented. This involves the interactive manipulation of ALP's being displayed on a color graphic screen. The ALP's are sets of grid points, denoting symbolic areas, lines, and points, committed to represent the physical structures, such as conductors, contacts, and FET's. Interactive features integrated into the design methodology include concurrent design rule checking, node labeling, and the resolution of design intentions as the designer is interactively composing symbolic circuit topology.

A mask geometries algorithm transforms the symbolic design into the precise mask set desired by any silicon foundry or fabricator. Each process is characterized to the mask geometries algorithm as a three-dimensional matrix. The matrix-elements define a geometrical attribute called SIZE, and context dependent attributes called COVER and PROTECT, which characterize the present state of a particular process-plant. An interactive editor provides a convenient means for creating or altering data to the mask geometries algorithm. The algorithm generates mask polygonal outlines which can be graphically examined by the designer or process engineer through a viewing window scaled to the desired perspective. A tracking ruler allows inter-mask and intra-mask feature measurements to be easily performed. This concept of mask generation provides an algorithmic form of design portability which enables symbolic design to be quickly and economically transported to any selected silicon foundry or fabricator.

SYMCAD incorporates a novel design analysis strategy that allows the designer to formulate many small problems, interactively posed one at a time. This strategy provides the timely tactical feedback to support the decision making process involved in the synthesis of high-performance devices. The circuit analysis function within SYMCAD is termed "Isolated Node Circuit Analysis (INCA)" while the logic simulation function is termed "Color Contrast Logic State Simulation (C2LS2)." Both these analysis

techniques utilize automatic model building algorithms that derive their respective models directly from the symbolic representation of the circuit topology to provide superior model completeness and fidelity. These interactive design analysis techniques are only partially developed at the present time and are not fully integrated into the SYMCAD design methodology.

6.2 SYMCAD DESIGN STATION

The hardware configuration defining the SYMCAD design station is shown in Figure 6.1 The software architecture supporting the SYMCAD design methodology is shown in Fig. 6.2. The central computational component is a DEC PDP-11/24 microcomputer supported by a Data Systems Winchester/ floppy disk memory system. The Winchester disk capacity is 7.8 megabytes and the floppy disk capacity is 1 megabyte. The major man-computer communications medium is a GENISCO GCT-6000 color graphic display. It is a 1024x1024 pixel, 5 plane, high resolution display with a 1:1 aspect ratio. The DEC VT-105 CRT display is used as a transaction log for designer monitoring.

The SYMCAD design station represents an affordable design station that can be economically replicated in each designer's office. This decentralization of CAD tools will improve designer productivity by technical enhancement and availability to perform design tasks. It also encourages an informality surrounding the performance of synthesis and analysis functions which stimulates creativity, by enabling routine evaluation of alternatives, and rapid exploration of candidate designs. It is deemed essential to develop this style of decentralized design environment to encourage and achieve high performance, high reliability device designs for military applications.

6.3 SYMCAD RELEVANCE TO GaAs TECHNOLOGY

SYMCAD can dramatically enhance the design methodology of GaAs devices in the future. It will influence the two salient design issues of circuit performance and designer productivity. In designing circuitry operating in the gigahertz range, circuit analysis techniques become a dominant influence in providing timely tactical feedback for effective decision making. SYMCAD utilizes a novel circuit analysis concept that allows the designer to pose many small problems, one at a time. Each problem is formulated as an isolated

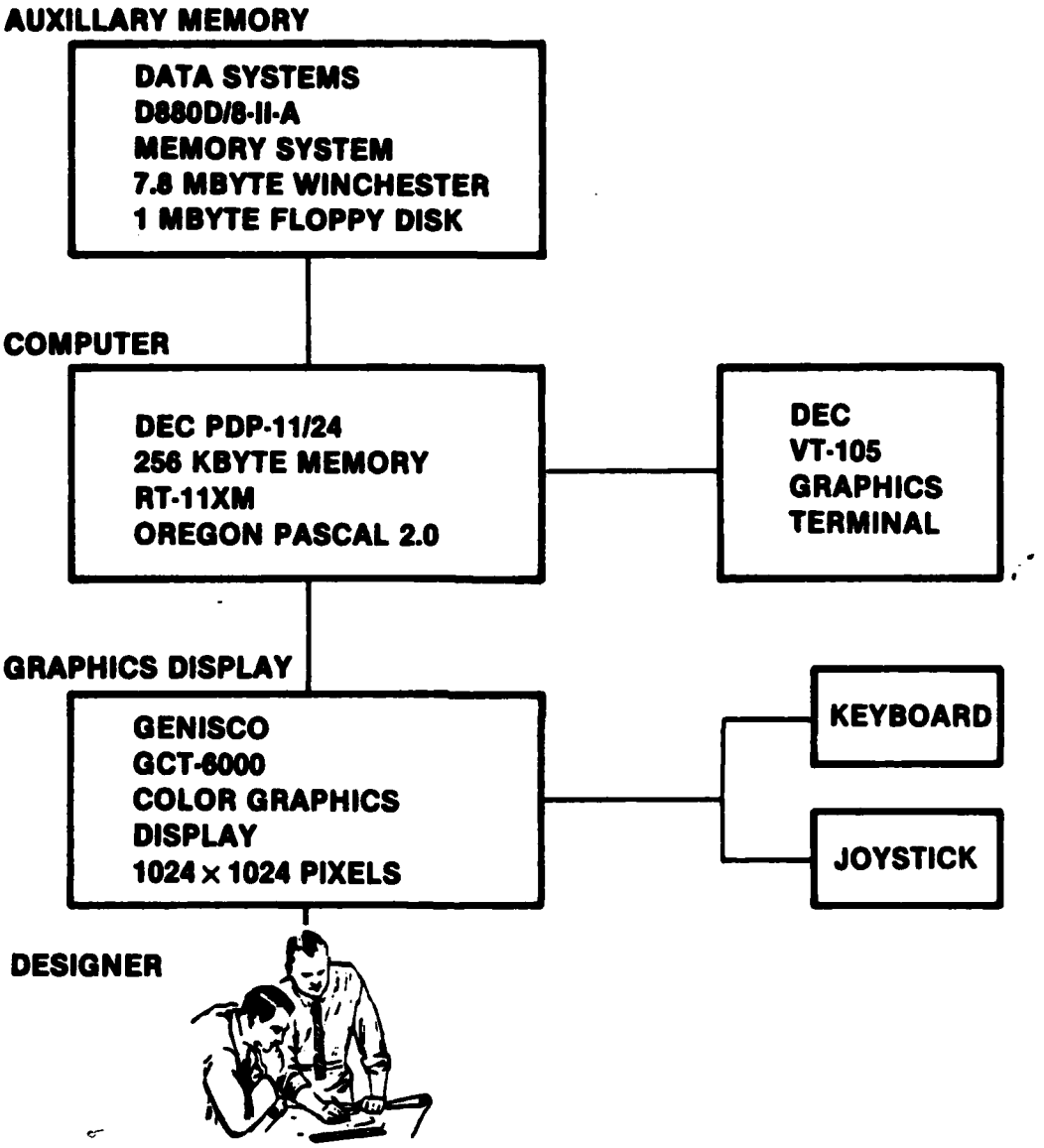


Figure 6.1 SYMCAD Design Station Configuration

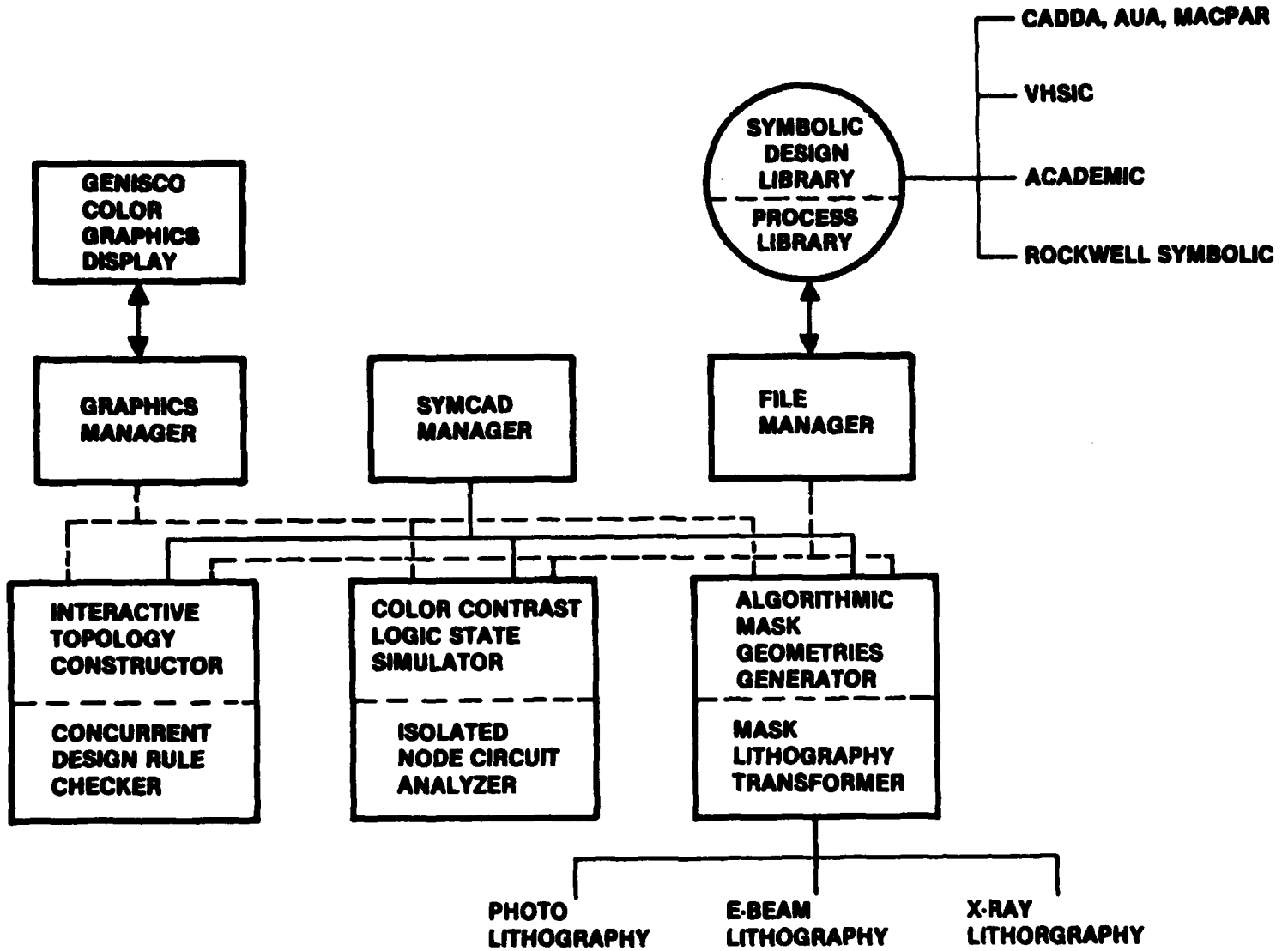


Figure 6.2 SYMCAD Software Architecture

node. The model of the isolated node is automatically derived from the symbolic representation of the circuit topology which provides model completeness superior to conventional manual derivation. The analytical solution is rapidly generated with the pictorial response displayed for immediate assessment. This interactive design style strengthens the synthesis process because it promotes exploration of alternatives.

SYMCAD possesses many unique concepts that will substantially contribute to improvement in designer productivity. The interactive composing of circuit topology using symbolic ALP's (areas, lines, points), in which the present state of the design is continuously displayed with color enhancement, is a simple means of capturing and documenting a design. The incorporation of a concurrent design rule checking technique during the composing procedure results in immediate detection of layout violations. Now corrective action can be pursued that will result in improved layout density. SYMCAD also utilizes a unique algorithmic technique for translating the symbolic design into a mask set whose geometries represent the present state of the process/plant. This results in the highest level of design portability attainable in transporting designs to the fabricator or silicon foundry. These productivity gains are an important aspect in striving to develop military applications maturity in GaAs technology.

The technical and economic relevance of SYMCAD to the GaAs technology can be summarized as illustrated in Fig. 6.3.

6.3.1 Short Term Relevance

The short term benefits which SYMCAD can provide in supporting the GaAs technology are:

1. Symbolic representation of circuit topology presented as color graphic display to designer.
2. Concurrent design rule checking throughout layout composition.
3. Node topology highlighting and surveying to aid in implementing optimal layout topology.
4. SIZE granularity in mask geometries generation.

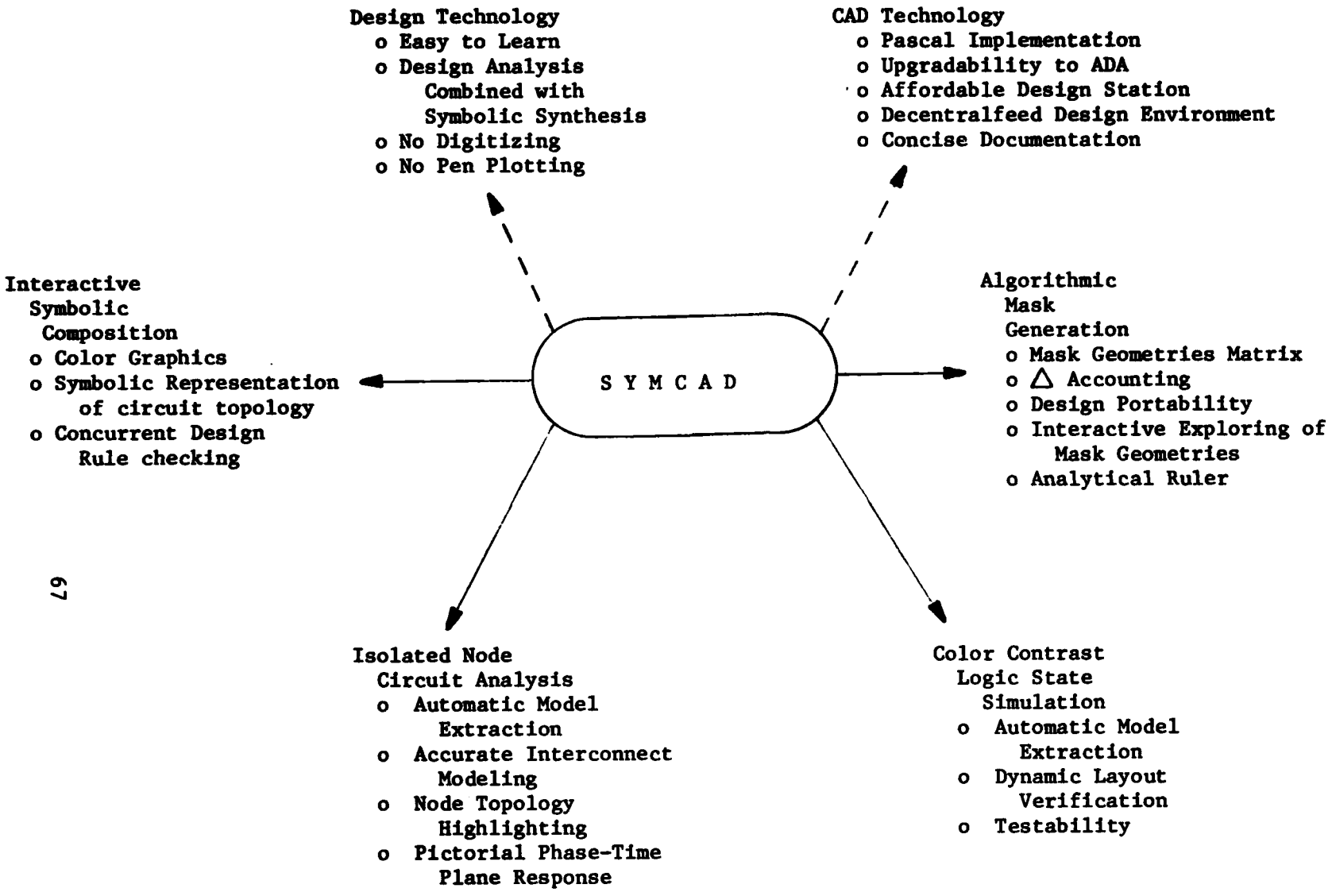


Figure 6.3 SYMCAD Properties Beneficial to GaAs Technology

5. Design portability using algorithmic mask geometries generation.

6. Improved designer productivity.

6.3.2 Long Term Relevance

The long term benefits which SYMCAD can provide in supporting the GaAs technology are:

1. Hierarchical symbolic design with supportive analysis.

2. Architectural planning aids for rapidly exploring alternative layout schemes.

3. Circuit analysis with model automatically derived from symbolic design for more completeness.

4. Dynamic layout verification using logic simulation with model automatically derived from symbolic design.

5. Hierarchical Interface Format (HIF) for servicing design-fabrication interface.

6.4 PROPOSED SYMCAD DEVELOPMENT FOR GaAs TECHNOLOGY

SYMCAD is not currently a completed symbolic design methodology. In its full realization, it possesses both horizontal and vertical dimensionality. That is, horizontal dimensionality refers to the development of an interactive symbolic design methodology which synergistically combines design analysis to support symbolic synthesis at the module level. The vertical dimensionality refers to the development of an interactive hierarchical symbolic design methodology to support device-level design. This will allow the designer to freely slide up and down the symbolic hierarchy in supporting top-down and bottom-up synthesis.

SYMCAD was developed using CMOS/SOS technology as a testing vehicle. Algorithmic and software extensions are required by GaAs technology because it uses more active elements and nonsymmetrical circuitry. Expansion of ALP-types will be required for symbolically representing resistors, diodes, MESFET's, and two metalization layers. Development of an Interactive Design Rules Matrix Editor would allow flexibility in characterizing design rules to the Concurrent Design Rules Checker. These new ALP-types will affect the Node Extraction Algorithm and the Automatic Model Builder used by design

analysis techniques; Isolated Node Circuit Analysis and Color Contrast Logic State Simulation. New macromodels for diodes and MESFET's must be incorporated into the Isolated Node Circuit Analyzer. The mask geometry requirements will demand more generalization in the Interactive Mask Geometries Matrix Editor and in the mask geometries algorithm.

The most urgent need is to provide SYMCAD with a hierarchical capability so that a device design may be composed representing a collection of modules with interconnections. The symbolic representation of modules as templates will allow the designer to place and manipulate outlines for architectural planning and implementation. The development of bus and interconnect routing macros will allow the designer to utilize regularity as a means of managing design complexity. The ability to invoke the Isolated Node Circuit Analysis technique to analyze interconnect structures in the planning stage is vital to GaAs technology with regard to maturity for military applications. The hierarchical characterization of the mask set to the fabricator must be developed to substantially reduce the volume of data currently being transported across the design-fabrication interface.

This proposed development program to enhance SYMCAD will result in an interactive symbolic design methodology that is ideally suited for the design and fabrication interfacing of GaAs devices. It will provide the economies necessary to realize high performance GaAs devices to be technology inserted into prototype military applications.

6.5 PROPOSED PHASE 1 SYMCAD DEVELOPMENT

6.5.1 Interactive Topology Constructor

6.5.1.1 ALP-Type Extensions

The present state of SYMCAD utilizes an ALP-type set appropriate for CMOS/SOS technology which utilizes complementary circuit configurations. However, the GaAs technology is considerably more complex. There are three predominant circuit configurations in GaAs; namely, depletion-mode logic (DFET), Schottky-diode FET logic (SDFL), enhancement-mode FET logic (ENFET). These circuit configurations have more passive and active circuit

elements than CMOS/SOS and use a two-layer metal interconnect scheme. Therefore, the number of ALP-types and their graphic representations must be increased as shown in Figure 6.4 for SDFL. Using these symbolic representations, the symbolic design for a GaAs NOR gate would be as shown in Fig. 6.5.

6.5.1.2 ALP-Sybtypes for Size Granularity

The mask geometries accompanying the GaAs technology requires much more granularity with regard to symbolic ALP's when compared to CMOS/SOS. The challenge in symbolic design is to minimize the number of ALP-types while maximizing the grid system scaling, called gamma. This reduces the symbolic complexity to a minimum thereby easing circuit interpretation and enhancing exploration and productivity.

SYMCAD currently uses ALP's in the context of a unique circuit function with a unique mask geometry size for each ALP. However, the GaAs technology, in its present state of development, will require ALP's to possess unique circuit function with many mask geometry sizes that are dependent on circuit configuration. By expanding SYMCAD's ALP-types to include subtypes, the circuit topological interpretation can remain simple while satisfying the mask geometry requirements for size granularity. This new feature of ALP-subtypes provides the mask geometries generation algorithm with additional mapping flexibility that can be selectively utilized when the technology demands it.

6.5.1.3 Develop DISTINGUISH Option

A new option, called DISTINGUISH, will be added to the Interactive Topology Constructor allowing the designer to graphically examine ALP-subtypes in this mode of operation.

6.5.1.4 Develop Interactive Design Rules Editor

As SYMCAD matures, there is a need to implement an interactive editor specifically developed to construct, modify, and document the design rules matrix characterizing a particular process. The present version of SYMCAD has the CMOS/SOS design rules matrix constructed at compile time which affords no flexibility to the process engineer or designer.

ALP - TYPE	SYMBOLIC ALP
bare GaAs	black
n+ doped conductor	green outline
cermet resistor	green ◆
saturated resistor	green ◇
logic diode	yellow ◉
level shift diode	green ●
MESFET	green ○
n+ - metal 1 contact	yellow ×
n+ - metal 2 contact	red ×
metal 1	yellow outline
metal 2	red outline
pad	red outline
reserved area	white outline

Figure 6.4 Symbolic Representations for a Typical GaAs Process (SDFL)

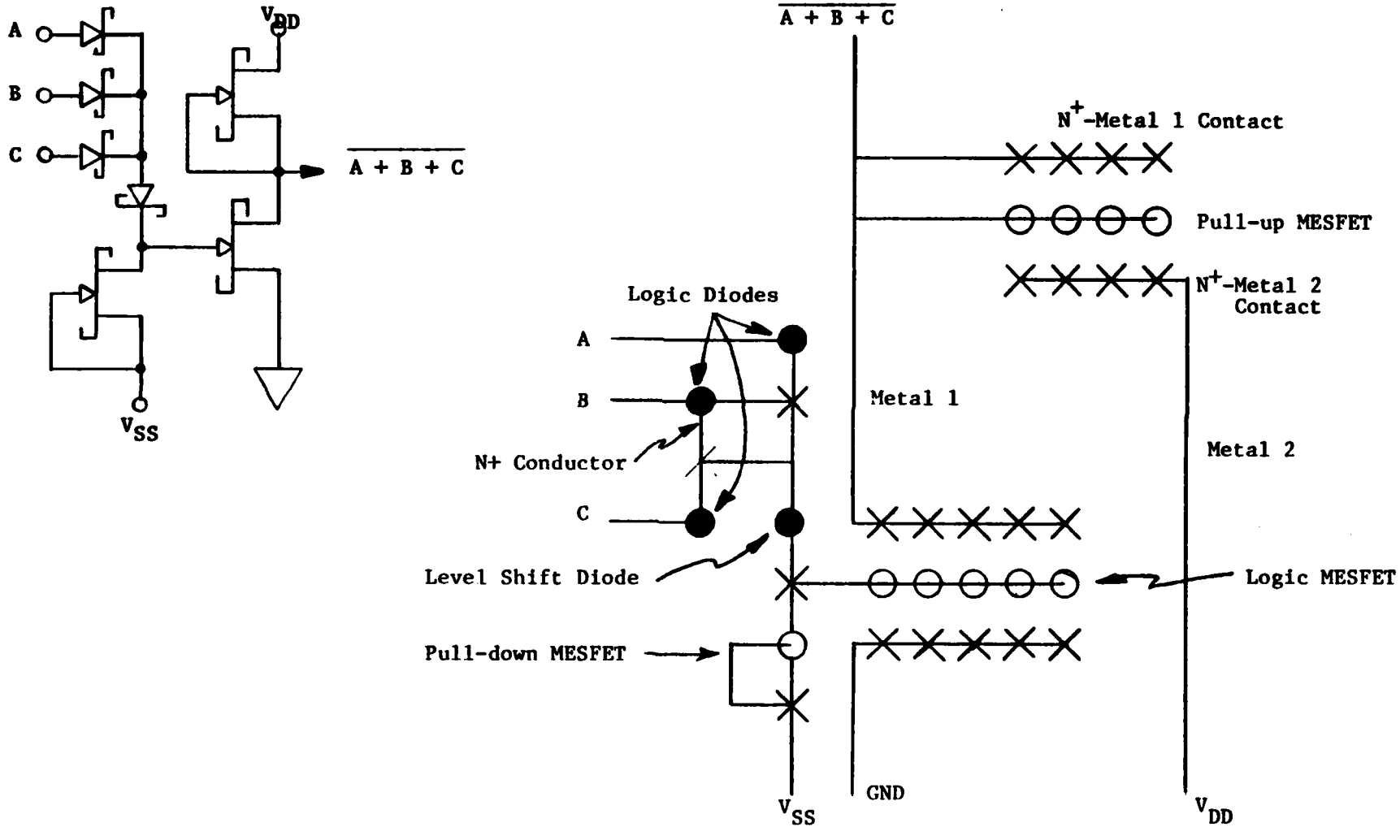


Figure 6.5 Symbolic Design of a GaAs NOR Gate (SDFL)

6.5.1.5 Expansion of Concurrent Design Rules Checker

The present version of SYMCAD demonstrated the technical and economical benefits of the Concurrent Design Rule Checker. It not only certifies the integrity of the design data base but also serves as a significant training aid. There is a need to generalize and modularize the existing software representing the Concurrent Design Rule Checker.

6.5.1.6 Expansion of CREATE, ERASE, JUGGLE Options

The CREATE, ERASE, and JUGGLE options need to be expanded to support the concept of ALP-subtypes. These are the major options used by the designer in composing symbolic circuit topology. The present versions of these options in SYMCAD are not fully developed and are significant contributors to improving designer productivity. A high-level node erase capability would be powerful in altering circuit topology. The JUGGLE, with its CUT and PASTE options, is also powerful in altering and replicating circuit topology involving collections of ALP's and needs to be fully implemented.

6.5.1.7 Restructuring of READ and WRITE DESIGN options

The file structure supporting the READ DESIGN and WRITE DESIGN options in the present version of SYMCAD need to be altered to capture the power of the variant record format capability in PASCAL. A file structure utilizing variant record formating will allow one file per module or device design with the CASE variable identifying the type of record. This file structure is better suited to support hierarchical symbolic design and eases file management activities being performed by the designer.

6.5.2 Algorithmic Mask Geometries Generator

6.5.2.1 Develop Gamma (Grid Scale) Optimizer

The development of the Gamma Optimizer is conceived as a front-end extension to the Interactive Mask Geometries Matrix Editor. It would allow the process engineer to mathematically describe the physical feature relationships of a process as a system of linear inequalities. Through the use of linear programming techniques, the process engineer can extremize

an optimizing function in deriving the optimal value for gamma - the symbolic scaling factor. Interactive techniques would allow the process engineer to easily construct the tableau and examine slack variables to determine criticality of physical feature constraints.

6.5.2.2 Extensions to Interactive Mask Geometries Matrix Editor

The Interactive Mask Geometries Matrix Editor in the present version of SYMCAD has demonstrated the flexibility needed in characterizing the present state of a process/plant. Software extensions will be needed for GaAs technology in constructing the SIZE and COVER/PROTECT planes comprising the Mask Geometries Matrix.

6.5.2.3 Algorithmic Enhancements for ALP-Subtypes

The Mask Geometries Generation Algorithm will be modified to process the new ALP-types and ALP-subtypes. The mask set for GaAs technology consists of fewer masks but the SIZE variations are broader than CMOS/SOS mask geometries. This mask geometries algorithm must be certified by generating mask sets for GaAs test vehicles.

6.5.2.4 SYMCAD Coupling to E-Beam Mask Lithography

A software package will be developed which will convert the SYMCAD polygonal mask geometries file into a format suitable for E-beam mask lithography processing at the U. S. Army ERADCOM facility and/or the Rockwell International facility.

6.6 PROPOSED PHASE 2 SYMCAD DEVELOPMENT

6.6.1 Automatic Model Builder

SYMCAD is committed to a degree of model completeness that far exceeds conventional modeling practices involving manual extraction procedures. To achieve this objective, an Automatic Model Builder concept is used to support both circuit analysis and logic simulation. An isolated node model, composed of a source-subgraph, sink-subgraph, and distribution-tree, is used as the common model component. An algorithmic procedure automatically derives the model directly from the symbolic design.

6.6.1.1 Expansion of Node Extraction Algorithm

GaAs technology introduces new circuit elements, such as resistors, diodes, and MESFET's, which will require modification to the Node Extraction Algorithm. The rules governing electrical contiguousness need to be expanded with no dramatic software modifications anticipated.

6.6.1.2 Development of Signal Flow Graph Model

The present version of SYMCAD does not automatically build the signal flow graph model used by the switch-level event simulator. The interactive graphical procedures for identifying input-output ports must be developed. A controlling algorithm for constructing the signal flow graph model must be developed in traversing form output port set to input port set by successive invoking of the Node Extraction Algorithm.

6.6.2 Isolated Node Circuit Analysis (INCA)

6.6.2.1 Develop Interactive Macromodeling Editor

An interactive editor capability needs to be developed which will tabulate the macromodeling parameters for active elements, e.g., diodes and MESFET's, and provide the macromodeling parameters for passive elements, e.g., conductor resistance and capacitive coupling to near neighbors.

6.6.2.2 Extensions to Node Surveyor

Continue development of the Node Surveyor for the GaAs technology environment to identify conductor couplings to neighboring conductors 1-gamma, 2-gamma, and 3-gamma distance away. Improve graphical presentation of coupling zones by tinting to indicated coupling strength related to capacitive value.

6.6.2.3 Develop Node Accountant

Develop an electrical parameter accounting scheme which will calculate the lumped parameter equivalents for the designated node under analysis. Explore the development of an innovative accounting scheme that calculates the unit electrical parameter values modeling each grid point within the topology comprising the node under analysis. A graphical presentation

must be developed to communicate these unit modeling values to the designer for assessment.

6.6.2.4 Develop Equations Formulator

An algorithmic procedure and dynamic data structure needs to be developed which will take the modeling parameters characterizing diodes, MESFET's, and interconnect structures and organize them in a suitable structure representing the coefficients of the nonlinear differential equations modeling the isolated node.

6.6.2.5 Adapt Equations Solver

An Adams-Moulton fourth order corrector-predictor integration algorithm has been developed and certified. Known enhancements need to be implemented to further reduce computation time and memory requirements. It is proposed to use this integration algorithm for GaAs circuit analysis and unite it to support the Equations Formulator.

6.6.3 Color Contrast Logic State Simulation (C2LS2)

6.6.3.1 Expansion of Model Exerciser

The Model Exerciser must be expanded to calculate state transitions for diodes and MESFET's. No changes to the quantized time accounting and event scheduling algorithm are anticipated.

6.6.3.2 Develop Graphic State Peruser

The Graphic State Peruser must be developed for C2LS2 to reach full conceptual maturity. Procedures and supporting algorithms must be developed to allow the designer to incrementally examine logic state behavior by coloring the symbolic node topology as a function of logic state at that particular instant in time.

6.7 PROPOSED PHASE 3 SYMCAD DEVELOPMENT

6.7.1 Interactive Architectural Planner

6.7.1.1 Develop Template Option

To support a hierarchical symbolic design environment, an option to allow the designer to characterize a module must be developed. In this hierarchical design structure, module designs will be treated as templates. A module template is a symbolic representation of a module that can be used for architectural planning of GaAs device designs. Each template contains the polygonal boundary, input-output port names, locations, and electrical-logic characteristics. In other words, the template is a high-level (symbolic) representation of a module. The data structure within SYMCAD must be altered to support this hierarchical representation of design entities.

6.7.1.2 Expand Manipulate Option for Module Templates

A preliminary version of a module template manipulation function currently exists in SYMCAD. It needs to be further refined so that the SYMCAD data structure is modified as template placement, reflection, rotation, copy, move, arraying, and erasure are graphically performed. This manipulation capability allows the designer to rapidly evaluate architectural schemes for functionality, signal flow, supply distribution, testability, and pad configuration.

6.7.1.3 Develop Bus Routing Macro

With a hierarchical symbolic design methodology that supports modularity and regularity, the major design tasks involve interconnect structures. Powerful macros must be developed to allow the designer to quickly create and modify interconnect and bus structures associated with signal nets. The SYMCAD data structure must support the hierarchical nature of interconnects since they can exist within and between modules.

6.7.1.4 Develop Pad/Scribe Line Generator

An algorithmic generator will be developed which will allow the designer to quickly view a pad and scribe line configurations referenced to the device outline.

6.7.2 Hierarchical Mask Composer

6.7.2.1 Module Declaration Section

The set of mask geometries defining each module in a device will be collected into a declaration section for each module.

6.7.2.2 Module Placement Section

A module placement section will contain the orientation and replication information for each module in a device. This information will allow the instantiation of mask geometries at a later time and results in a significant reduction of data volume when regularity has been used in the device architecture.

6.7.2.3 Hierarchical Interface Format (HIF) for Hierarchical Symbolic Design

The intrinsic hierarchical structure of a device design will be preserved into a mask geometries data structure appropriate for interfacing into the mask lithography facility. This data structure will be known as the Hierarchical Interface Format (HIF). This will allow the instantiated representation of mask geometries to be performed within the mask fabricator's facility. HIF fully embraces the concepts of algorithmic design portability being advocated by SYMCAD.

6.8 ESTIMATED PROGRAM RESOURCES

Table XII. presents the resources estimated to perform the development of the major GaAs enhancements to SYMCAD. This schedule is for planning purposes only and is not to be construed as implying any contractual commitment by Rockwell International.

This SYMCAD development program assumes 42 manmonths effort spread over a 24 month time span.

TABLE XII. SYMCAD PROGRAM SCHEDULE

Tasks	Year 1				Year 2			
	1	2	3	4	1	2	3	4
PHASE 1 PROGRAM								
Topology Constructor (6 MM)	—							
Mask Generation (8 MM)		—						
PHASE 2 PROGRAM								
INCA (12 MM)				—	—	—		
C2LS2 (6 MM)							—	—
PHASE 3 PROGRAM								
Architectural Planner (6 MM)		—						
Mask Composer (4 MM)			—					

*MM - Man Months

6.9 SYMCAD RELATED BIBLIOGRAPHY

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